Semi-High
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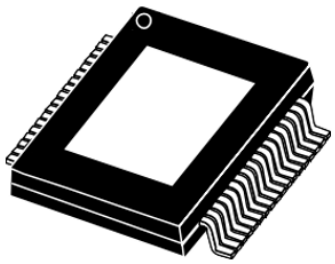
SMH7492E

79 W + 79 W dual BTL class-D audio



Features

- Wide-range single-supply operation (7 - 26 V)
- Possible output configurations:
  - 2 x PBTL
  - 1 x Parallel BTL
- BTL output capabilities (VCC = 26 V):
  - 61 W + 61 W, 4 Ω, THD 1%
  - 79 W + 79 W, 4 Ω, THD 10%
  - 45 W + 45 W, 6 Ω, THD 1%
  - 56 W + 56 W, 6 Ω, THD 10%
  - 37 W + 37 W, 8 Ω, THD 1%
  - 46 W + 46 W, 8 Ω, THD 10%
- Parallel BTL output capabilities (VCC = 26 V):
  - 91 W, 3 Ω, THD 1%
  - 114 W , 3 Ω, THD 10%
- High efficiency
- Four selectable, fixed-gain settings of nominally 20.4 dB, 26.4 dB, 29.9 dB and 32.4dB
- Differential inputs minimize common-mode noise
- Standby, mute and play operating modes
- Short-circuit protection
- Output power limited by PLMIT function
- Detection of shorted output pins during startup
- Thermal overload protection

Description

The SMH7492E is a dual BTL class-D audio amplifier with single power supply designed for home audio applications.

The device is housed in a 28-pin TSSOP package with exposed pad up (EPU), and as a result of its high efficiency, a simple heatsink is required.

Applications

- Multimedia Speaker
- Aftermarket Automotive
- Sound Bar and Boombox

Table 1.Device summary

Order code	Operating temp. range	Package	Packaging
SMH7492E	-40 to +85°C	E-TSSOP28	Tape and reel

79 W + 79 W dual BTL class-D audio

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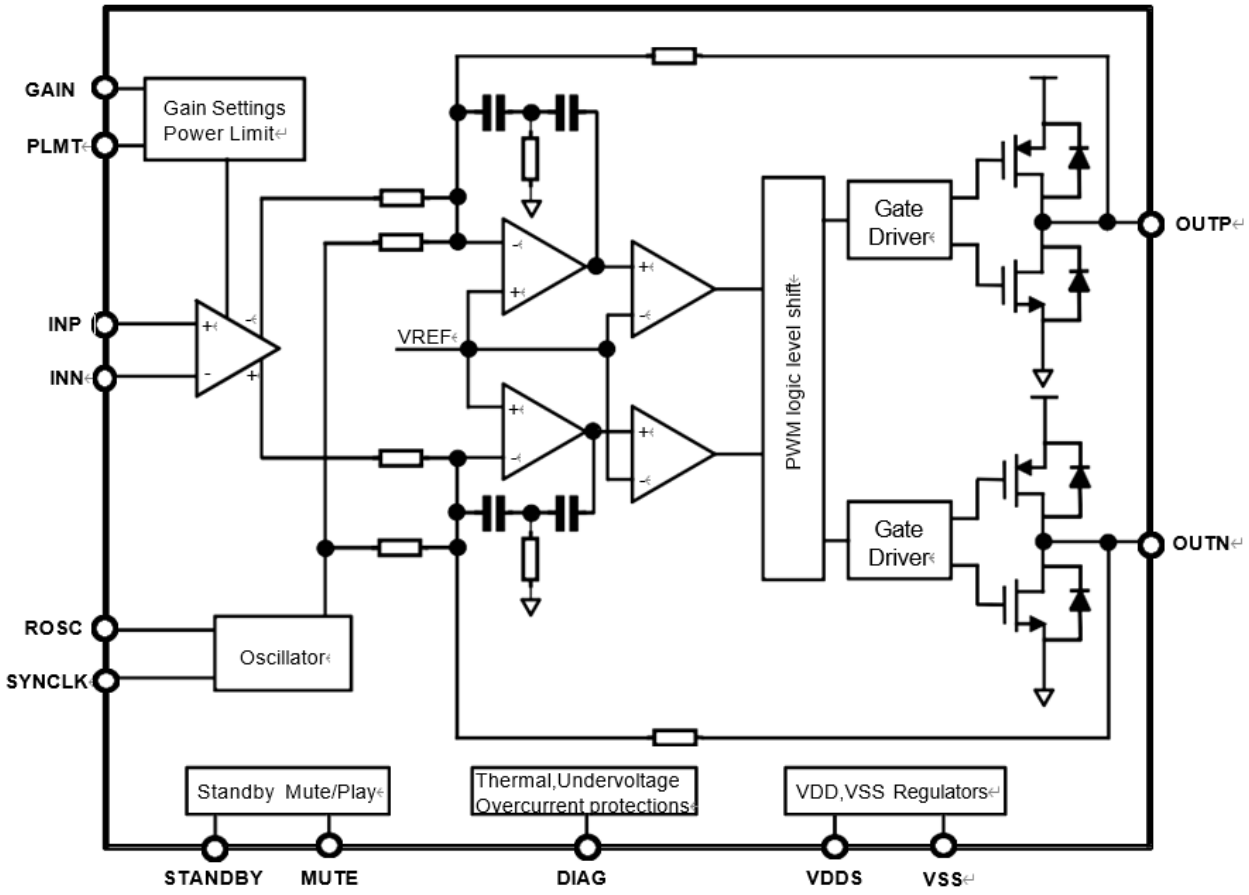
1. Device block diagram

Figure 1. Internal block diagram (showing one channel only) shows the block diagram of one of the two identical channels of the SMH7492E.

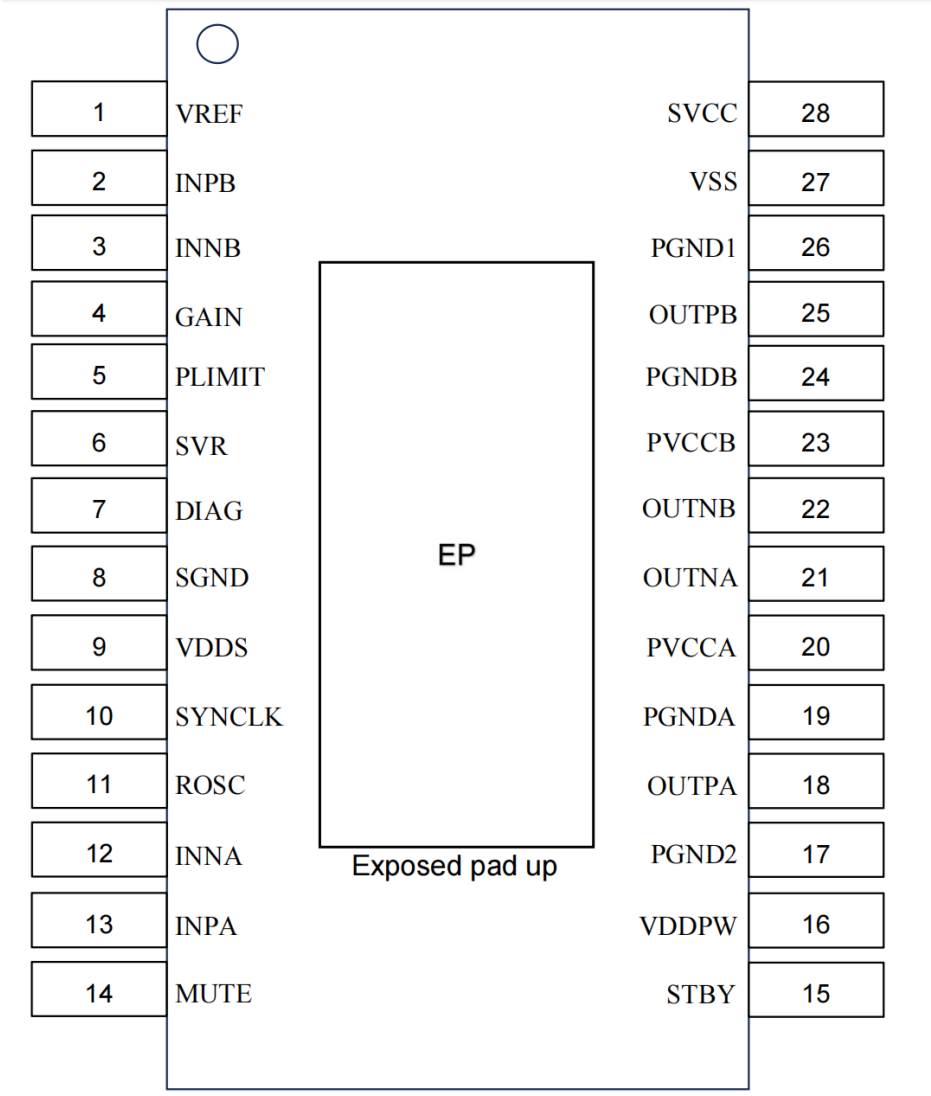
Figure 1.Internal block diagram (showing one channel only



2. Pin description

2.1 Pinout

Figure 2.Pin connections (top view, PCB view)



2.2 Pin list

Table 2.Pin description list

Pin Number	Name	Type	Description
1	VREF	O	Half VDDS (nominal) referred to ground
2	INPB	I	Positive differential input of right channel
3	INNB	I	Negative differential input of right channel
4	GAIN	I	Gain setting
5	PLIMIT	I	Limit different maximum power
6	SVR	O	Supply voltage rejection
7	DIAG	O	Open-drain diagnostic output
8	SGND	PWR	Signal ground
9	VDDS	O	3.3-V (nominal) regulator output referred to ground for signal blocks
10	SYNCLK	I/O	Clock in/out for external oscillator
11	ROSC	O	Master oscillator frequency-setting pin
12	INNA	I	Negative differential input of left channel
13	INPA	I	Positive differential input of left channel
14	MUTE	I	Mute mode control
15	STBY	I	Standby mode control
16	VDDPW	O	3.3-V (nominal) regulator output referred to ground for power stage
17	PGND	PWR	Power stage ground
18	OUTPA	O	Positive PWM output for left channel
19	PGNDA	PWR	Power stage ground for left channel
20	PVCCA	PWR	Power supply for left channel
21	OUTNA	O	Negative PWM output for left channel
22	OUTNB	O	Negative PWM output for right channel
23	PVCCB	PWR	Power supply for right channel
24	PGNDB	PWR	Power stage ground for right channel
25	OUTPB	O	Positive PWM for right channel
26	PGND	PWR	Power stage ground
27	VSS	O	3.3-V (nominal) regulator output referred to power supply
28	SVCC	PWR	Signal power supply

3. Absolute maximum ratings

Table 3.Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCMAX}	DC supply voltage for pins PVCCA, PVCCB, SVCC	30	V
VI	Voltage limits for input pins STANDBY, MUTE, INNA, INPA, INNB, INPB, GAIN	-0.3 to 5	V
T_{op}	Operating temperature	-40 to 85	°C
T_j	Junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

4. Thermal data

Table 4.Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient	-	24 (1)	-	°C/W

5. Electrical specifications

Unless otherwise stated, the results in Table 5: "Electrical specifications" below are given for the conditions: VCC = 26 V, RL= 6 Ω, ROSC = 39 kΩ, f = 1 kHz, GV = 20.4 dB and Tamb = 25 °C.

Table 5.Electrical specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage for pins PVCCA, PVCCB, SVCC	-	7	-	26	V
I_q	Total quiescent current	Without LC, no load	-	40		mA
I_{qSTBY}	Quiescent current in standby	-	-	1	-	µA
V_{OS}	Output offset voltage	Vi = 0, Av = 20 dB, no load		20		mV
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	9	10	13	A
T_j	Junction temperature at thermal shutdown	-	140	150	160	°C
R_i	Input resistance	Differential input		60	-	kΩ
R_{dsON}	Power transistor on-resistance	High side	-	0.35	-	Ω
		Low side	-	0.25	-	
G_V	Closed-loop gain	GAIN4 < 0.25*Vdd		20.4	-	dB
		0.25*Vdd < GAIN3 < 0.5*Vdd	-	26.4	-	
		0.5*Vdd < GAIN2 < 0.75*Vdd	-	29.9	-	
		GAIN1>0.75*Vdd	-	32.4	-	
ΔG_V	Gain matching	-	-	-	±1	dB
CT	Crosstalk	f = 1 kHz	-	80	-	dB
PSRR	Power supply voltage rejection ratio		-	-	-	dB
T_r, T_f	Rise and fall times	PWM signal 50% duty cycle	-	24	40	ns
f_{SW}	Switching frequency	Internal oscillator with external Rosc = 39 kΩ	-	420	-	kHz
f_{SWR}	Output switching frequency range	With internal oscillator by changing Rosc (1)	420	-	550	kHz
V_{inH}	Digital input high (H)	-	2.0	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
Function mode	Standby, Mute, Play	STBY < 0.5 V Mute = 'X'	Standby			
		STBY > 2.5 V Mute < 0.8 V	Mute			
		STBY > 3 V Mute > 2.5 V	Play			
A_{MUTE}	Mute attenuation	V_{MUTE} = 1 V	60	80	-	dB

Notes: $f_{SW} = 10^6 / [(12 * R_{OSC} + 110) * 4]$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ (where R_{OSC} is in kΩ and f_{SW} in kHz) with Rosc = 39 kΩ.

5.1 Stereo BTL application

All specifications are for VCC = 26 V, Rosc = 39 kΩ, f = 1 kHz, Tamb = 25 °C, unless otherwise specified.

Table 6.Stereo BTL application

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_o	Output power	R_L = 6 Ω, THD = 10%	-	56	-	W
		R_L = 6 Ω, THD = 1%	-	45	-	
		R_L = 4 Ω, THD = 10%	-	79	-	
		R_L = 4 Ω, THD = 1%	-	61	-	
THD	Total harmonic distortion	P_o = 1 W, fin = 1 kHz R_L = 6 Ω	-	0.04	-	%
		P_o = 1 W, fin = 1 kHz R_L = 4 Ω		0.08		
VN	Total output noise	Inputs shorted and connected to GND, A curve, G_V = 20.4 dB	-	150	-	μV

5.2 Parallel BTL(mono) application

All specifications are for VCC = 22 V, Rosc = 30 kΩ, f = 1 kHz, Tamb = 25 °C, unless otherwise specified.

Table 7.Stereo BTL(mono) application

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_o	Output power	R_L = 3 Ω, THD = 10%	-	90	-	W
		R_L = 3 Ω, THD = 1%	-	71	-	
		RL = 3 Ω, THD = 10% Vcc = 26V	-	118	-	
		RL = 3 Ω, THD = 1% Vcc = 26V	-	92	-	
THD	Total harmonic distortion	P_o = 1 W, fin = 1 kHz R_L = 3 Ω	-	0.13	-	%
VN	Total output noise	Inputs shorted and connected to GND, A curve, G_V = 20.4 dB	-	150	-	μV

6. Applications circuit

Figure 3.Applications circuit for class-D amplifier (BTL)

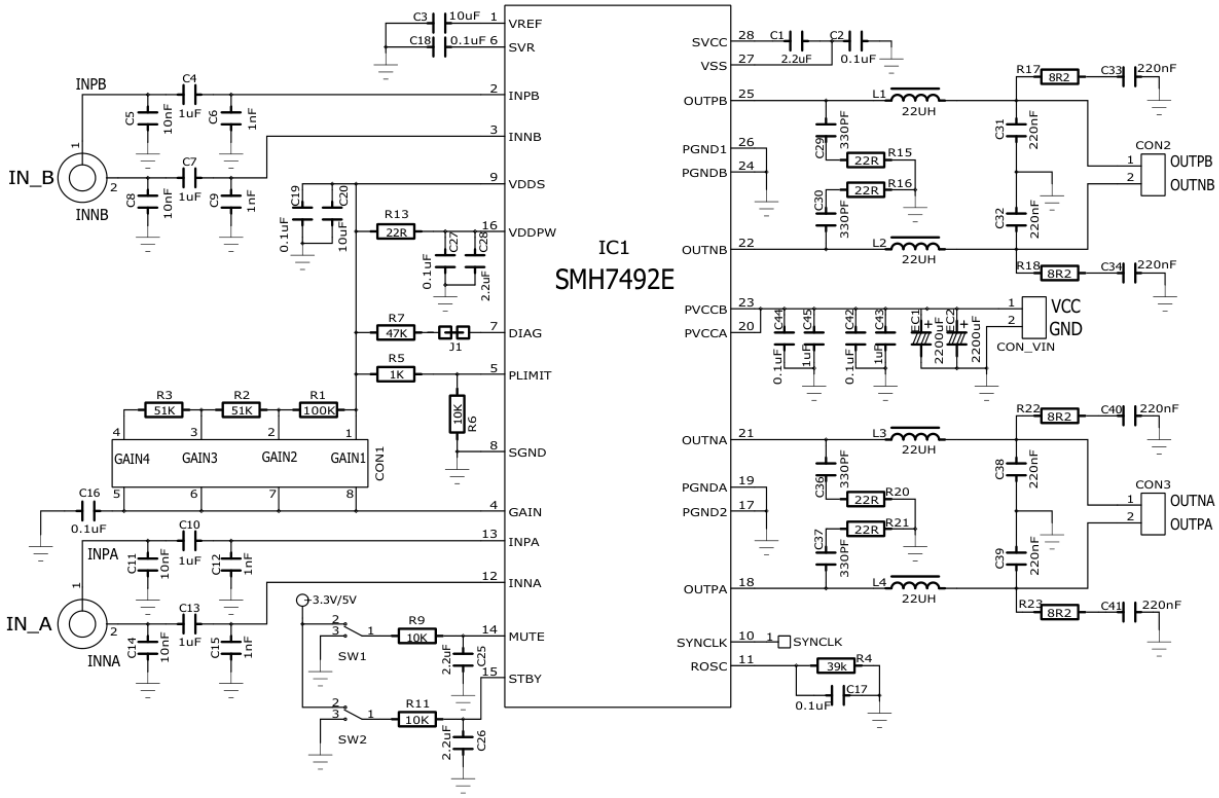


Figure 4. Applications circuit for class-D amplifier (PBTL)

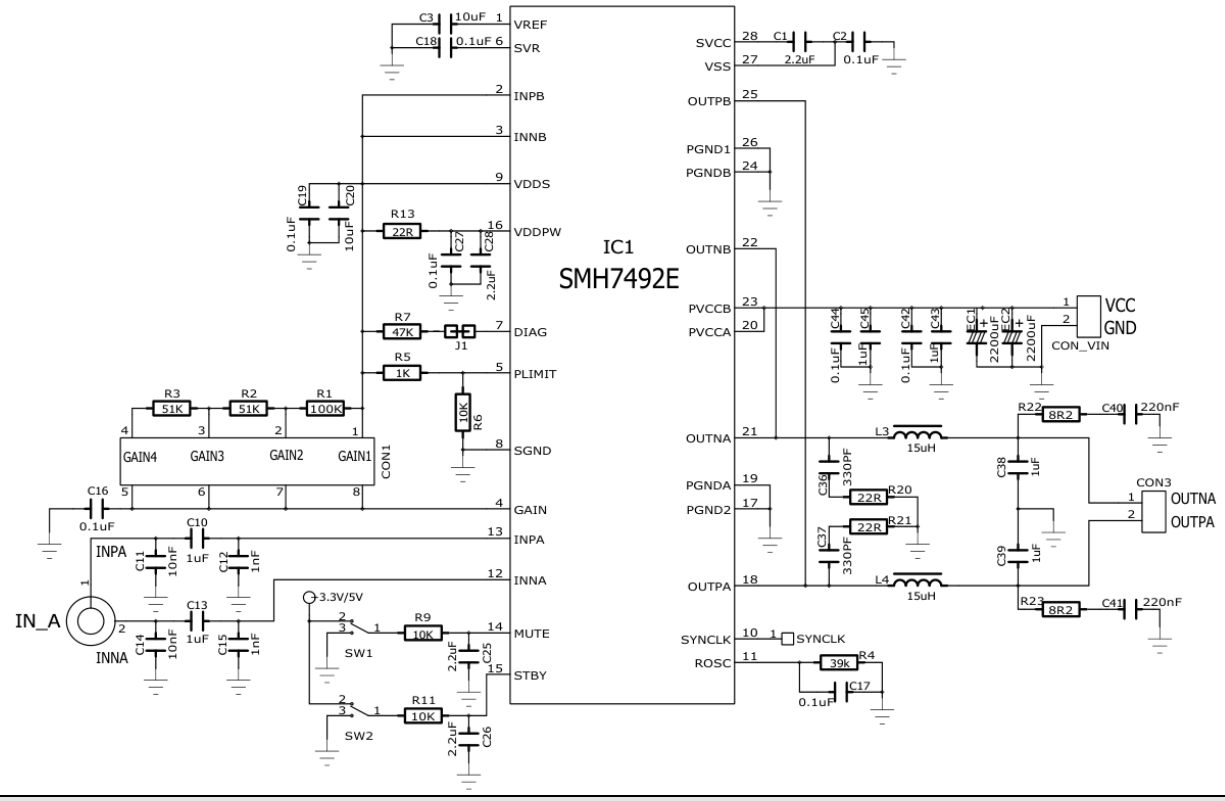
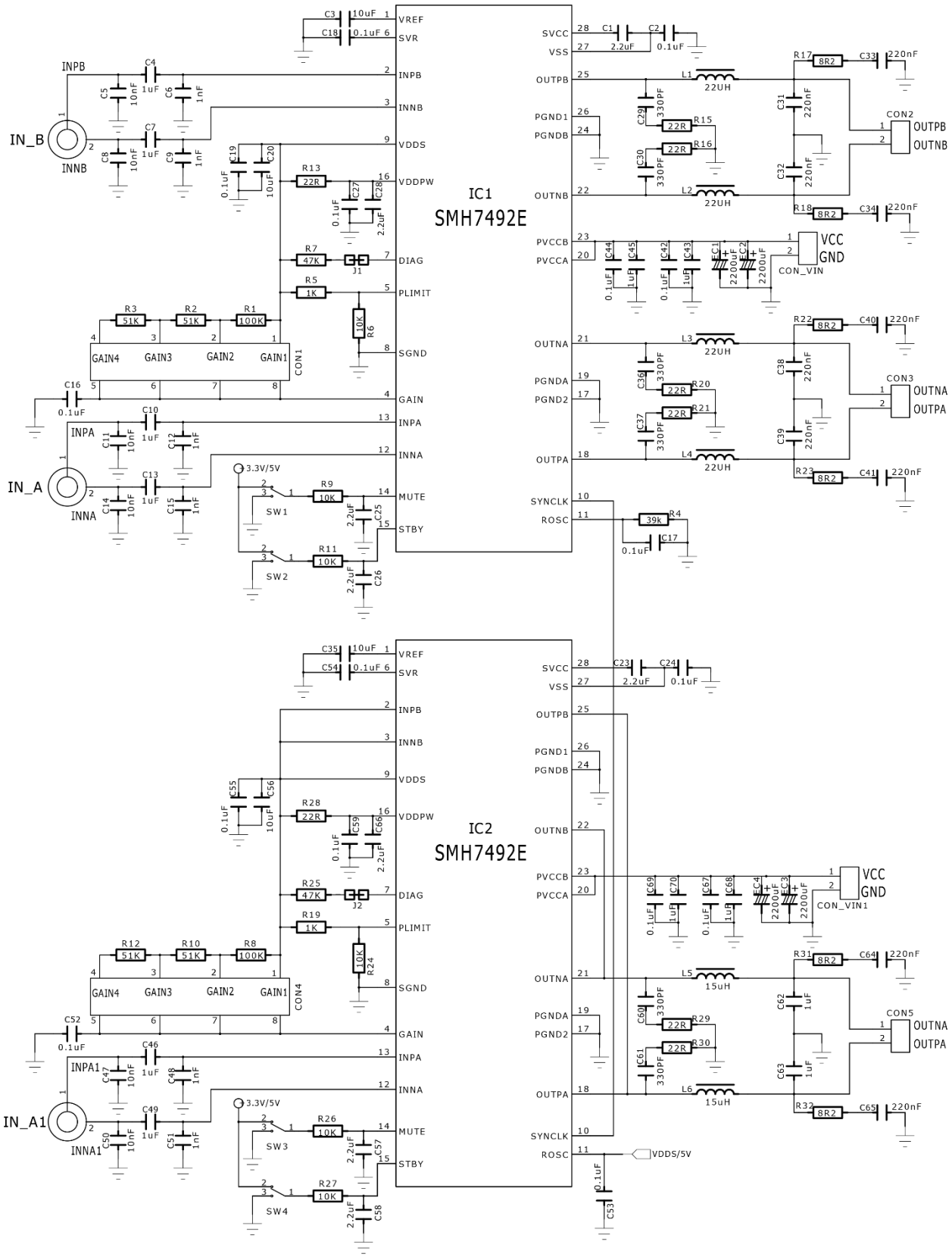


Figure 5. Applications circuit for class-D amplifier (BTL+PBTL)



7. Characterization curves

Unless otherwise stated, measurements were made under the following conditions: VCC = 26 V, Rl = 6 Ω, f = 1 kHz, Gv = 32.4 dB, Rosc = 39 kΩ, Tamb = 25 °C.

Note: Maximum output power must be derated according to case temperature.

7.1 Stereo configuration

The following characterization curves were made using the SMH7492E demonstration board (Figure 3: "Application circuit"). The characterization curves were made under the following test conditions:

Vs = 7 and 26 V, Rl = 6 Ω, Rosc = 39 kΩ, Cosc = 100 nF, Gain = 32.4 dB and Tamb = 25°C unless otherwise specified.

Figure 6. Efficiency vs output power

(Vs = 26 V, RL = 2 x 6 ohm, f = 1kHz)

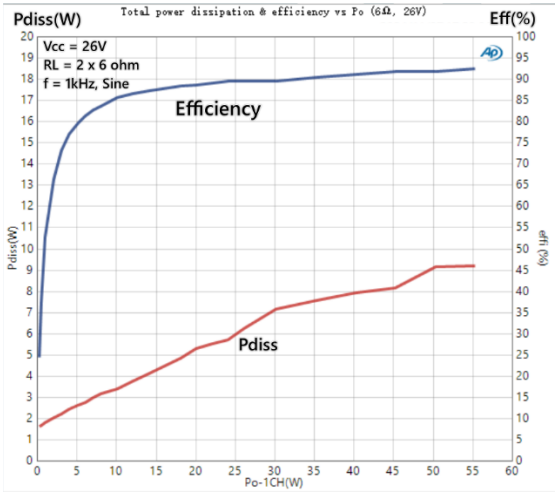


Figure 7. Efficiency vs output power

(Vs = 20V, RL = 2 x 6 ohm, f = 1kHz)

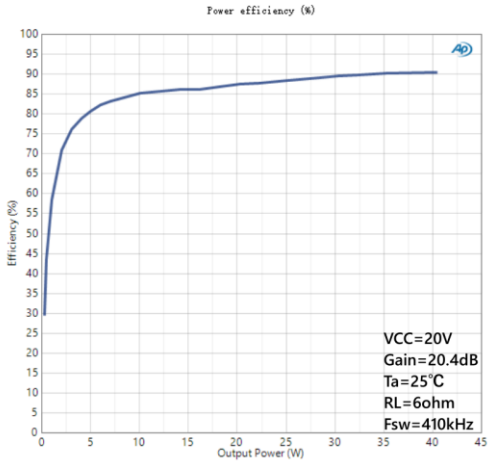


Figure 8. Efficiency vs output power

(RL = 2 x 4 ohm, f = 1kHz Gain = 26dB)

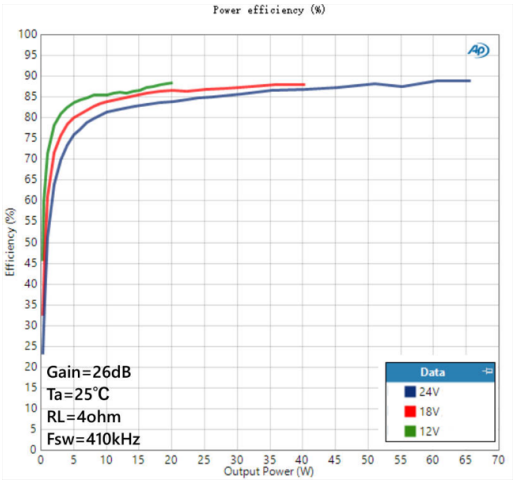


Figure 9.THD vs Pout

(Vs = 26 V, f = 1 kHz)

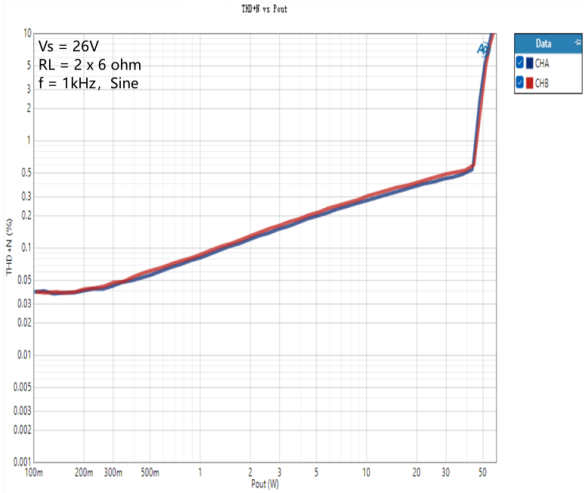


Figure 10. THD vs Pout

(Vs = 26 V, f = 100 Hz)

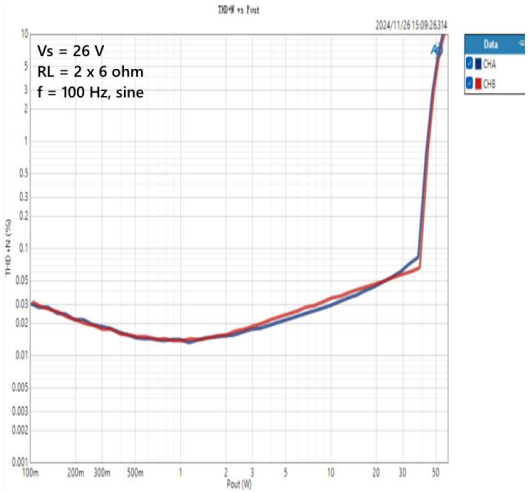


Figure 11. THD vs Pout

(Vs = 26 V, f = 6 kHz)

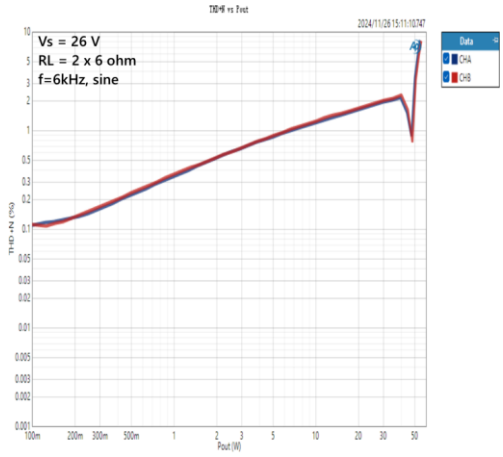


Figure 12. THD vs frequency

(Vs = 26 V, Po = 1 W)

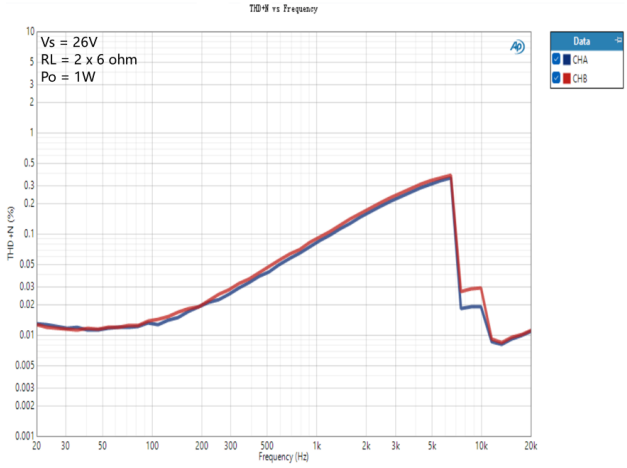


Figure 13. Crosstalk (Vs = 26 V)

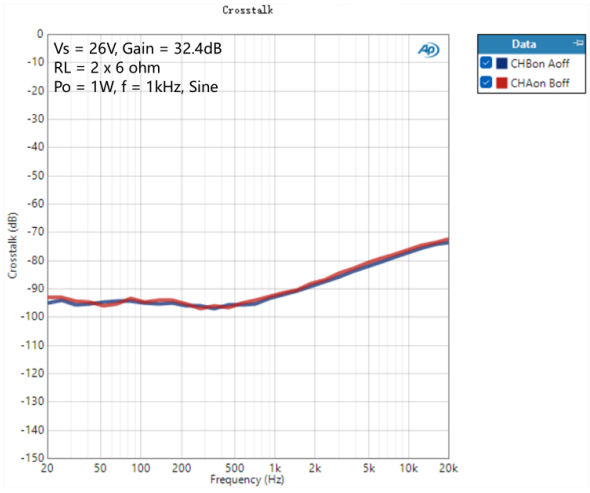


Figure 14. FFT (0 dB) (Vs = 26 V)

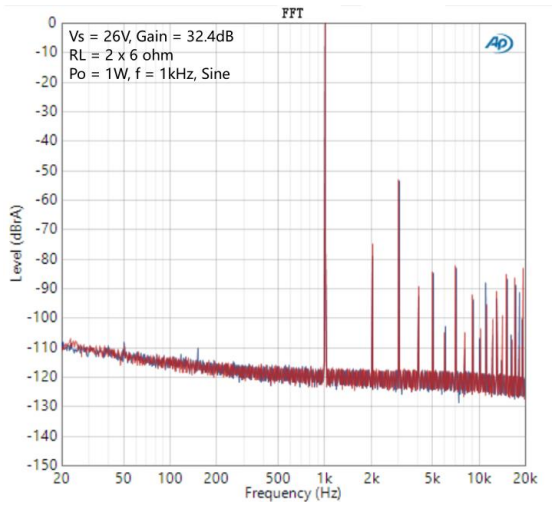
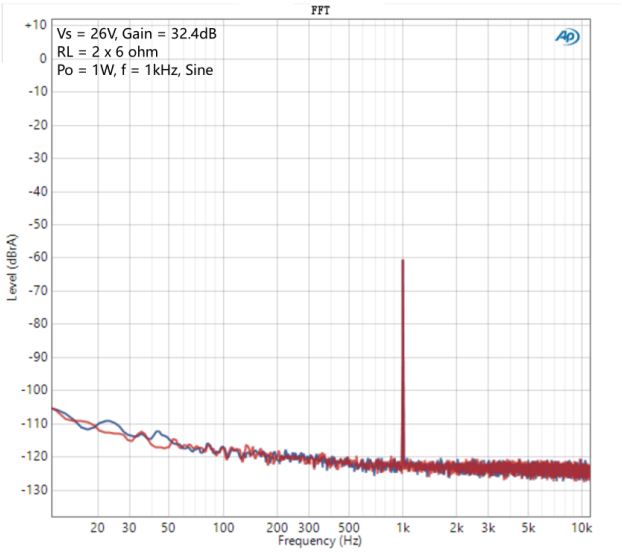


Figure 15. FFT (-60 dB) (Vs = 26 V)



8. Applications information

8.1 Mode selection

The three operating modes of the SMH7492E are set by the two inputs STBY (pin 15) and MUTE (pin 14).Standby mode: all circuits are turned off, very low current consumption.

- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the SMH7492E are enabled by pulling down the voltages of the STBY and MUTE inputs shown in Figure 13. The input current of the corresponding pins must be limited to 200 µA.

Table 8. Mode settings

Mode selection	STBY	MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Drive levels defined in *Table 5: Electrical specifications on page 6*

Figure 16.Standby and mute circuits

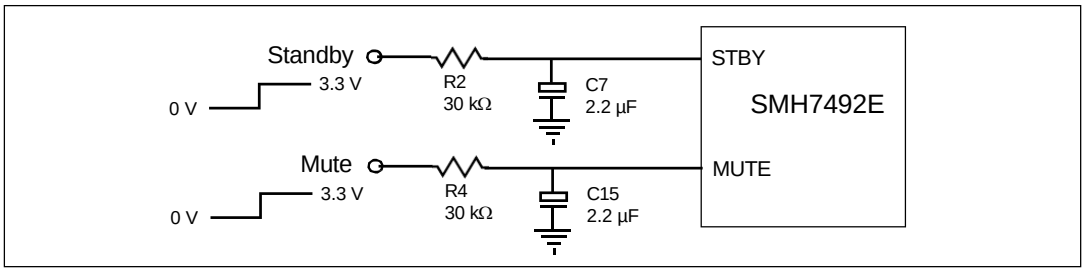
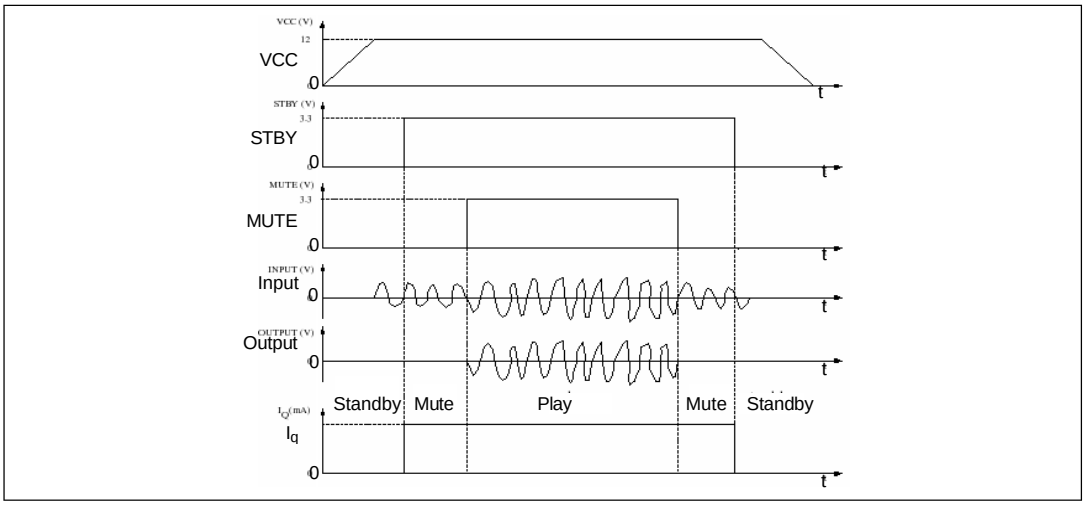


Figure 17.Turn-on/off sequence for minimizing speaker "pop"



8.2 Gain setting

The gain of the SMH7492E is setting by changing the feedback resistors of the amplifier.

Table 9.Gain settings

GAIN	Nominal gain, G_v (dB)
1	32.4
2	29.9
3	26.4
4	20.4

8.3 Input resistance and capacitance

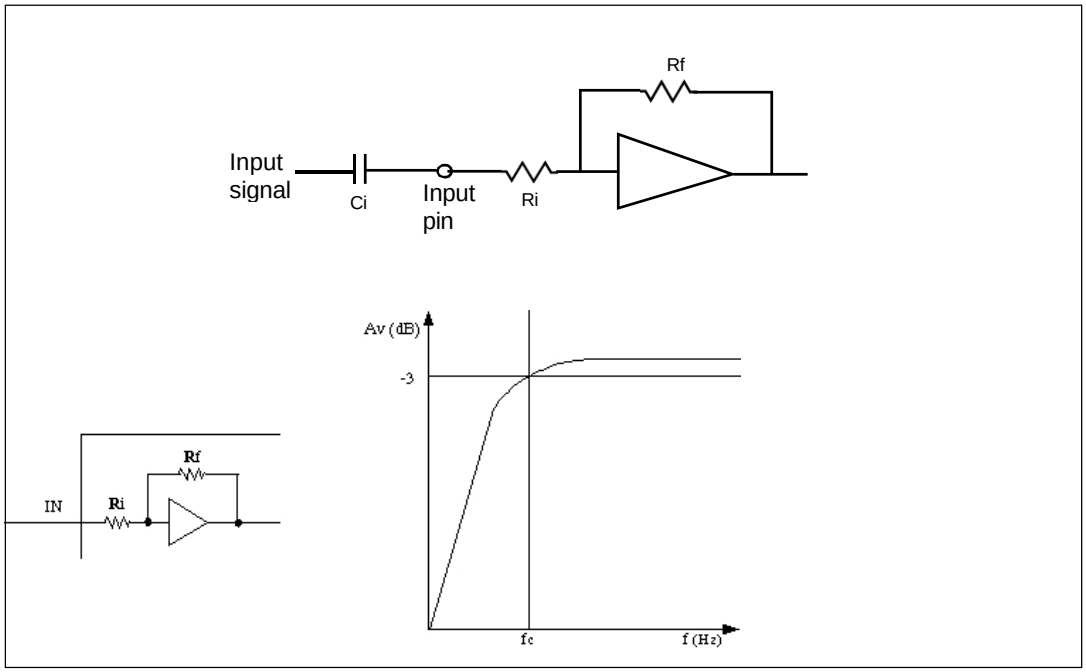
The input impedance is set by an internal resistor Ri = 60 kΩ (typical). An input capacitor (Ci) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in

Figure 15. For Ci = 470 nF the high-pass filter cutoff frequency is below 20 Hz:

fc = 1 / (2 * pi * Ri * Ci)

Figure 18.Device input circuit and frequency response



8.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one SMH7492P as master clock, while the other devices are in slave mode (that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

8.5 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW}, is controlled by the resistor, Rosc, connected to pin ROSC: $f_{SW} = 10^6 / ((16 * R_{OSC + 182}) * 4)$ kHz where R_{OSC} is in 39 kΩ.

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is: $f_{SYNCLK} = 2 * f_{SW}$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 kΩ as given below in Table 9.

8.6 Slave mode (external clock)

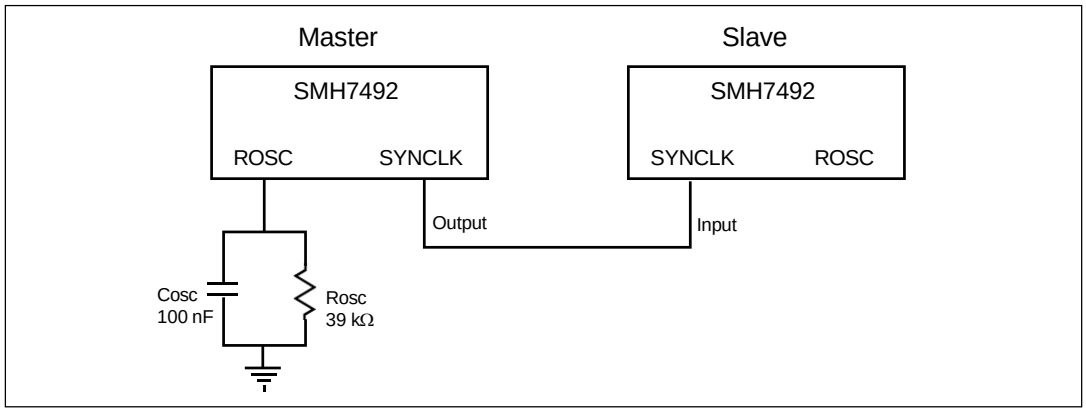
In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in Table 10.

The output switching frequency of the slave devices is: $f_{SW}=f_{SYNCLK} / 2$.

Table 10.How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	R_{OSC} < 60 kΩ	Output
Slave	Floating (not connected)	Input

Figure 19.Master and slave connection



8.7 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cutoff frequency of 27 kHz, are shown in Figure 17 and Figure 18 below.

Figure 20. Typical LC filter for a 8Ω speaker

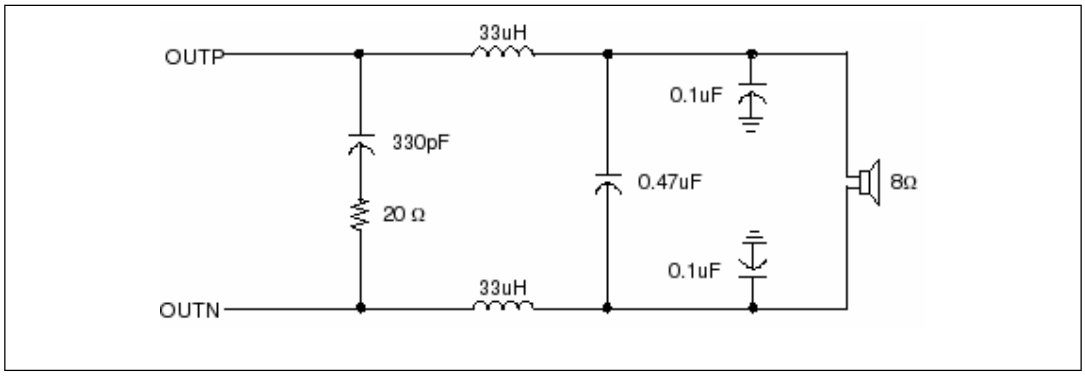
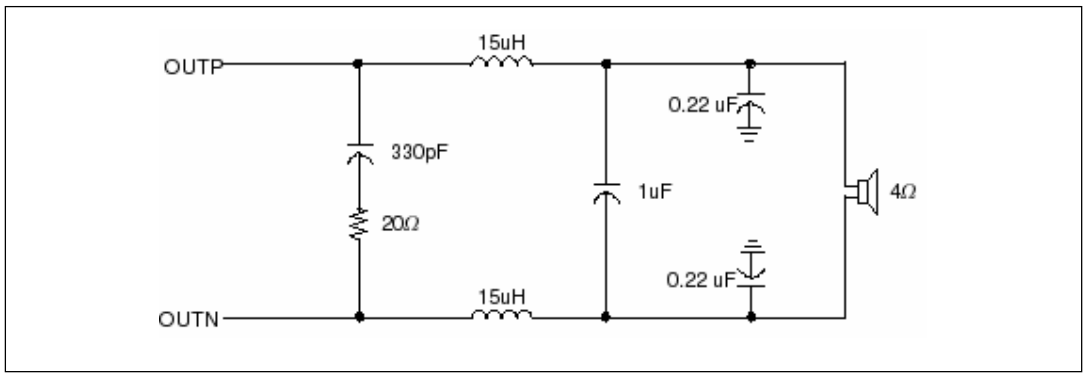


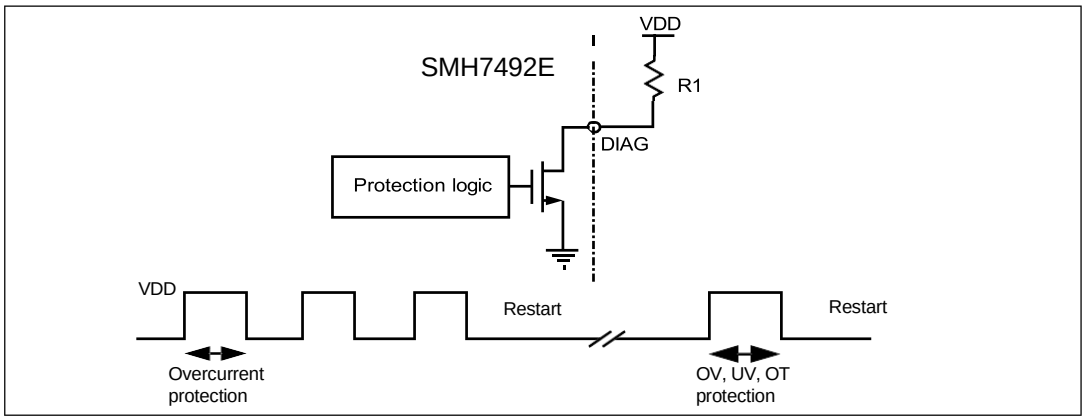
Figure 21.Typical LC filter for a 4Ω speaker



8.8 Diagnostic output

The output pin DIAG is an open-drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<26 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 µA) of the pin.

Figure 22. Behavior of pin DIAG for various protection conditions



9. Protection functions

The SMH7492E is fully protected against overvoltage, undervoltage, overcurrent and thermal overloads as explained here.

Overvoltage protection (OVP)

If the supply voltage exceeds the value for VOVP given in Table 5: Electrical specifications on page 8 the overvoltage protection is activated which forces the outputs to the

high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

Undervoltage protection (UVP)

If the supply voltage drops below the value for VUVP given in Table 5: Electrical specifications on page 8 the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value for IOCP given in Table 5: Electrical specifications on page 8 the overcurrent protection is activated which forces the outputs to the

high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, TOC, is determined by the R-C components connected to pin STBY.

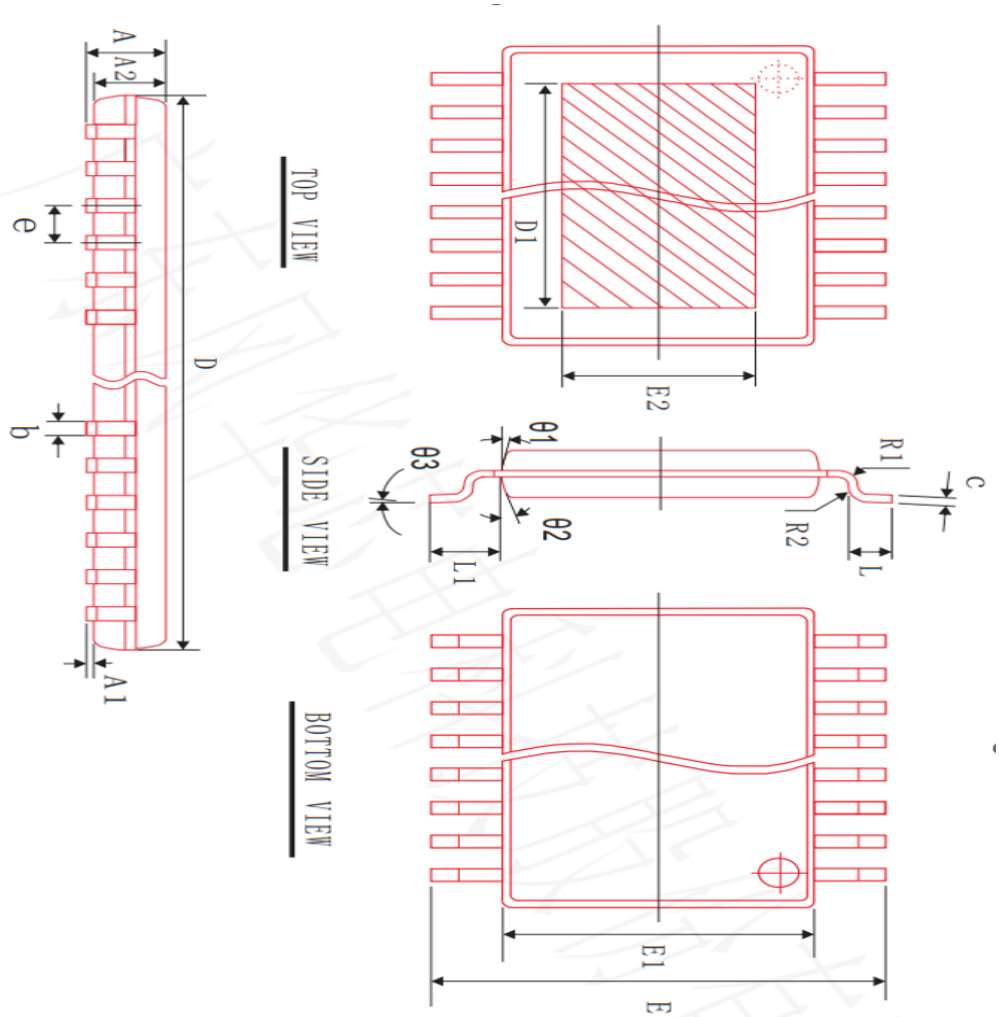
Thermal protection (OTP)

If the junction temperature, Tj, reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for Tj given in Table 5: Electrical specifications on page 8 the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently the device restarts.

10. Package mechanical data

The SMH7492E comes in a 28-pin E-TSSOP28 package with exposed up.

Figure 23.TSSOP28 package outline



COMMON DIMENSIONS (UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	---	---	1.20
A1	0.05	0.10	0.15
A2	0.80	0.875	1.05
c	0.09	0.145	0.20
b	0.19	0.255	0.30
L1	0.95	1.00	1.05
L	0.45	0.60	0.75
D1	5.80	5.90	6.00
E2	2.90	3.00	3.10
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
D	9.60	9.70	9.80
θ3	0	4	8
R1	0.15 TYP		
R2	0.15 TYP		
θ1	0.12°TYP		
θ2	0.12°TYP		
e	0.65 BSC		

11. Revision history

Table 11.Document revision history

Date	Revision	Changes
15-Aug-2024	1.0	Initial release.
20-Aug-2024	1.1	Add the internal block diagram and Update the Pin description
25-Nov-2024	1.2	Update the Electrical specifications and Modify some formats
28-Nov-2024	1.3	Update the application circuit
30-Nov-2024	1.4	Add the Characterization curves and Update the application circuit
9-Dec-2024	1.5	Add application
11-Dec-2024	1.6	Update the Characterization curves
13-Dec-2024	1.7	Update the Features and Add Parallel BTL(mono) application
16-Dec-2024	1.8	Update the application circuit
17-Dec-2024	1.9	Update the Application circuit and the Characterization curves
10-Jan-2025	2.0	Update the Pin list

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