

## 45 W + 45 W dual BTL class-D audio amplifier

### Features

- Wide-range single-supply operation (7 - 26 V)
- Possible output configurations:
  - 2 x BTL
  - 1 x Parallel BTL
- BTL output capabilities (VCC = 26 V):
  - 45 W + 45 W, 4 Ω, THD 1%, VCC 22V
  - 61 W + 61 W, 4 Ω, THD 1%, VCC 26V
  - 45 W + 45 W, 6 Ω, THD 1%, VCC 26V
  - 56 W + 56 W, 6 Ω, THD 10%, VCC 26V
  - 37 W + 37 W, 8 Ω, THD 1%, VCC 26V
  - 46 W + 46 W, 8 Ω, THD 10%, VCC 26V
- High efficiency
- Four selectable, fixed-gain settings of nominally 20.4 dB, 26.4 dB, 29.9 dB and 32.4dB
- Differential inputs minimize common-mode noise
- Standby, mute and play operating modes
- Short-circuit protection
- Output power limited by PLMIT function
- Detection of shorted output pins during startup
- Thermal overload protection

### Description

The SMH7492PE is a dual BTL class-D audio amplifier with single power supply designed for home audio applications.

The device is housed in a 28-pin TSSOP package with exposed pad down and as a result of its high efficiency.

### Applications

- Multimedia Speaker
- Aftermarket Automotive
- Sound Bar and Boombox

**Table 1. Device summary**

Order code	Op Temp	Package	Package Qty	Mark
SMH7492PE	-40 to +85°C	TSSOP28	4000	SMH7492PE xxxxxxx xxx

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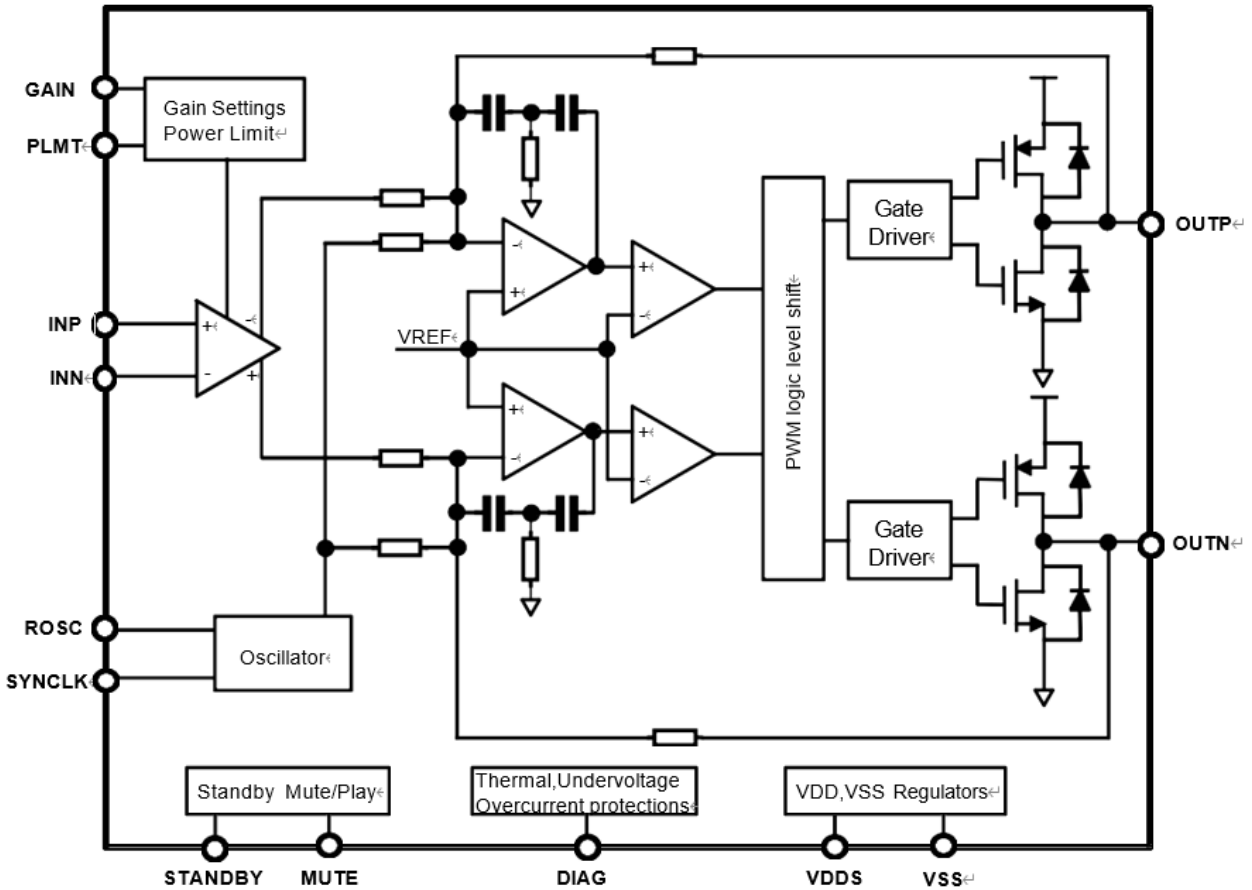
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## 1. Device block diagram

Figure 1. Internal block diagram (showing one channel only) shows the block diagram of one of the two identical channels of the SMH7492PE.

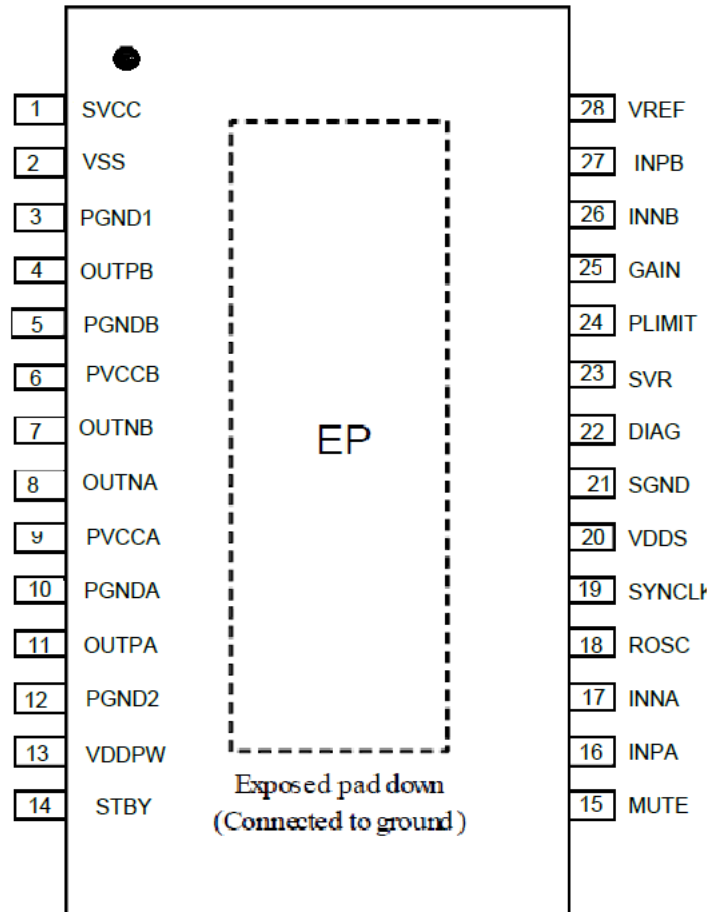
Figure 1. Internal block diagram (showing one channel only)



## 2. Pin description

### 2.1 Pinout

Figure 2.Pin connections (top view, PCB view)



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**2.2 Pin list**
**Table 2.Pin description list**

Pin Number	Name	Type	Description
1	SVCC	PWR	Signal power supply
2	VSS	O	3.3-V (nominal) regulator output referred to power supply
3	PGND	PWR	Power stage ground
4	OUTPB	O	Positive PWM for right channel
5	PGNDB	PWR	Power stage ground for right channel
6	PVCCB	PWR	Power supply for right channel
7	OUTNB	O	Negative PWM output for right channel
8	OUTNA	O	Negative PWM output for left channel
9	PVCCA	PWR	Power supply for left channel
10	PGNDA	PWR	Power stage ground for left channel
11	OUTPA	O	Positive PWM output for left channel
12	PGND	PWR	Power stage ground
13	VDDPW	O	3.3-V (nominal) regulator output referred to ground for power stage
14	STBY	I	Standby mode control
15	MUTE	I	Mute mode control
16	INPA	I	Positive differential input of left channel
17	INNA	I	Negative differential input of left channel
18	ROSC	O	Master oscillator frequency-setting pin
19	SYNCLK	I/O	Clock in/out for external oscillator
20	VDDS	O	3.3-V (nominal) regulator output referred to ground for signal blocks
21	SGND	PWR	Signal ground
22	DIAG	O	Open-drain diagnostic output
23	SVR	O	Supply voltage rejection
24	PLIMIT	I	Limit different maximum power
25	GAIN	I	Gain setting
26	INNB	I	Negative differential input of right channel
27	INPB	I	Positive differential input of right channel
28	VREF	O	Half VDDS (nominal) referred to ground

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### 3. Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CCMAX}$	DC supply voltage for pins PVCCA, PVCCB, SVCC	30	V
$V_I$	Voltage limits for input pins STANDBY, MUTE, INNA, INPA, INN B, INPB, GAIN	-0.3 to 5	V
$T_{op}$	Operating temperature	-40 to 85	°C
$T_j$	Junction temperature	-40 to 150	°C
$T_{stg}$	Storage temperature	-40 to 150	°C

### 4. Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j-case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j-amb}$	Thermal resistance, junction to ambient	-	24 <sup>(1)</sup>	-	°C/W



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## 5. Electrical specifications

Unless otherwise stated, the results in Table 5: "Electrical specifications" below are given for the conditions:  $V_{CC} = 26\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $R_{OSC} = 39\text{ k}\Omega$ ,  $f = 1\text{ kHz}$ ,  $G_V = 20.4\text{ dB}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

**Table 5. Electrical specifications**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply voltage for pins PVCCA, PVCCB, SVCC	-	7	-	26	V
$I_q$	Total quiescent current	Without LC, no load	-	40		mA
$I_{qSTBY}$	Quiescent current in standby	-	-	1	-	$\mu\text{A}$
$V_{OS}$	Output offset voltage	$V_i = 0$ , $A_v = 20\text{ dB}$ , no load		20		mV
$I_{OCP}$	Overcurrent protection threshold	$R_L = 0\ \Omega$	9	10	13	A
$T_j$	Junction temperature at thermal shutdown	-	140	150	160	$^\circ\text{C}$
$R_i$	Input resistance	Differential input		60	-	k $\Omega$
$R_{dsON}$	Power transistor on-resistance	High side	-	0.15	-	$\Omega$
		Low side	-	0.1	-	
$G_V$	Closed-loop gain	$GAIN4 < 0.25 * V_{dd}$		20.4	-	dB
		$0.25 * V_{dd} < GAIN3 < 0.5 * V_{dd}$	-	26.4	-	
		$0.5 * V_{dd} < GAIN2 < 0.75 * V_{dd}$	-	29.9	-	
		$GAIN1 > 0.75 * V_{dd}$	-	32.4	-	
$\Delta G_V$	Gain matching	-	-	-	$\pm 1$	dB
CT	Crosstalk	$f = 1\text{ kHz}$	-	80	-	dB
PSRR	Power supply voltage rejection ratio		-	-	-	dB
$T_r, T_f$	Rise and fall times	PWM signal 50% duty cycle	-	24	40	ns
$f_{sw}$	Switching frequency	Internal oscillator with external $R_{osc} = 39\text{ k}\Omega$	-	420	-	kHz
$f_{swR}$	Output switching frequency range	With internal oscillator by changing $R_{osc}$ <sup>(1)</sup>	420	-	550	kHz
$V_{inH}$	Digital input high (H)	-	2.0	-	-	V
$V_{inL}$	Digital input low (L)		-	-	0.8	
Function mode	Standby, Mute, Play	$STBY < 0.5\text{ V}$ Mute = 'X'	Standby			
		$STBY > 2.5\text{ V}$ Mute $< 0.8\text{ V}$	Mute			
		$STBY > 3\text{ V}$ Mute $> 2.5\text{ V}$	Play			
$A_{MUTE}$	Mute attenuation	$V_{MUTE} = 1\text{ V}$	60	80	-	dB

Notes:  $f_{sw} = 10^6 / [(12 * R_{osc} + 110) * 4]\text{ kHz}$ ,  $f_{sYNCLK} = 2 * f_{sw}$  (where  $R_{osc}$  is in k $\Omega$  and  $f_{sw}$  in kHz) with  $R_{osc} = 39\text{ k}\Omega$ .

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**5.1 Stereo BTL application**

All specifications are for  $V_{CC} = 26\text{ V}$ ,  $R_{osc} = 39\text{ k}\Omega$ ,  $f = 1\text{ kHz}$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 6. Stereo BTL application**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$P_o$	Output power	$R_L = 6\ \Omega$ , THD = 10%	-	56	-	W
		$R_L = 6\ \Omega$ , THD = 1%	-	45	-	
		$R_L = 4\ \Omega$ , THD = 10%	-	79	-	
		$R_L = 4\ \Omega$ , THD = 1%	-	61	-	
THD	Total harmonic distortion	$P_o = 1\text{ W}$ , $f_{in} = 1\text{ kHz}$ $R_L = 6\ \Omega$	-	0.04	-	%
		$P_o = 1\text{ W}$ , $f_{in} = 1\text{ kHz}$ $R_L = 4\ \Omega$	-	0.08	-	
VN	Total output noise	Inputs shorted and connected to GND, A curve, $G_v = 20.4\text{ dB}$	-	150	-	$\mu\text{V}$

**5.2 Parallel BTL (mono) application**

All specifications are for  $V_{CC} = 22\text{ V}$ ,  $R_{osc} = 33\text{ k}\Omega$ ,  $f = 1\text{ kHz}$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , INPB, INNB connected to VDDS, unless otherwise specified.

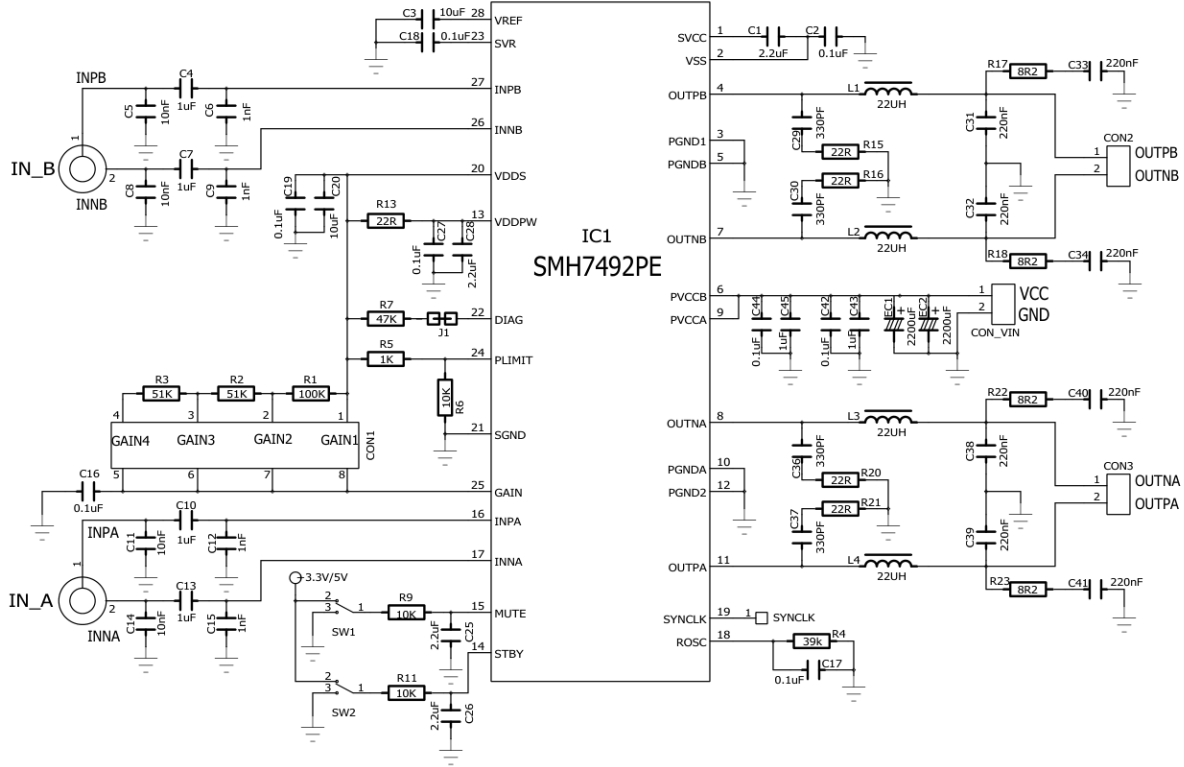
**Table 7. Stereo BTL (mono) application**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$P_o$	Output power	$R_L = 3\ \Omega$ , THD = 10%	-	90	-	W
		$R_L = 3\ \Omega$ , THD = 1%	-	71	-	
		$R_L = 3\ \Omega$ , THD = 10% $V_{cc} = 18\text{ V}$	-	53	-	
		$R_L = 3\ \Omega$ , THD = 1% $V_{cc} = 18\text{ V}$	-	41	-	
THD	Total harmonic distortion	$P_o = 1\text{ W}$ , $f_{in} = 1\text{ kHz}$ $R_L = 3\ \Omega$	-	0.05	-	%
VN	Total output noise	Inputs shorted and connected to GND, A curve, $G_v = 20.4\text{ dB}$	-	150	-	$\mu\text{V}$

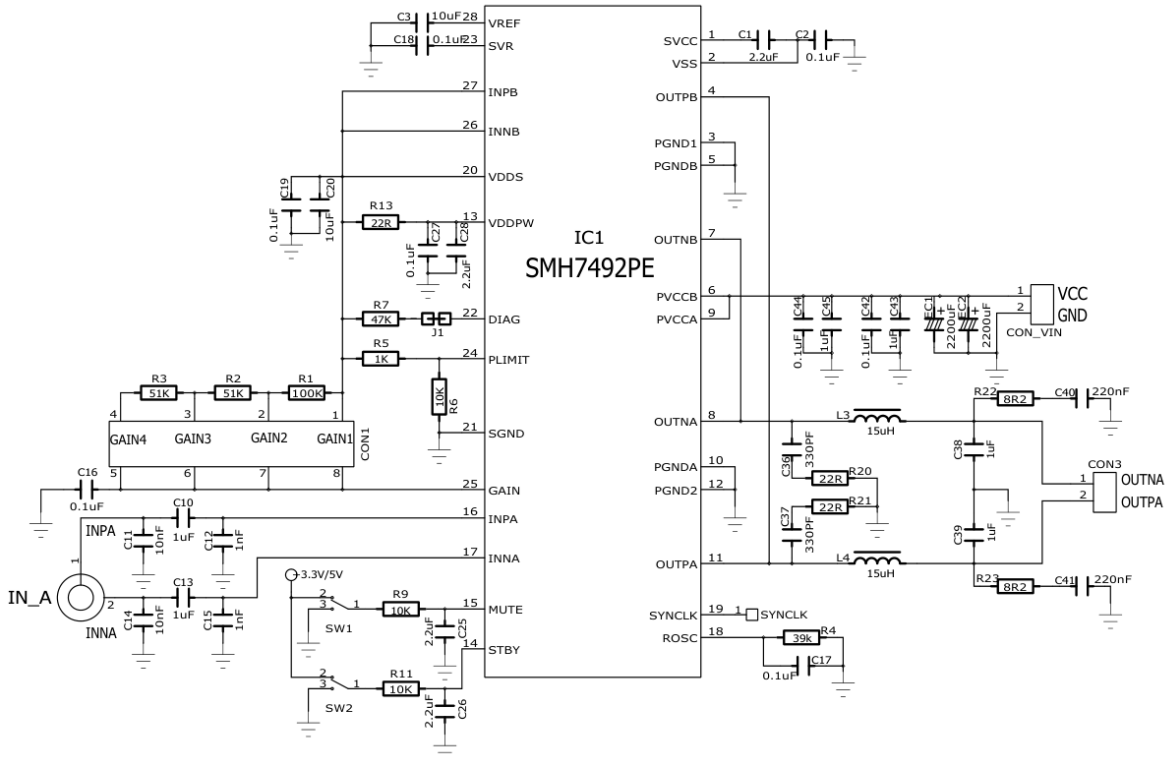
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**6. Applications circuit**

**Figure 3. Applications circuit for class-D amplifier(BTL)**



**Figure 4. Applications circuit for class-D amplifier(PBTL)**





**45 W + 45 W dual BTL class-D audio amplifier**

**7. Characterization curves**

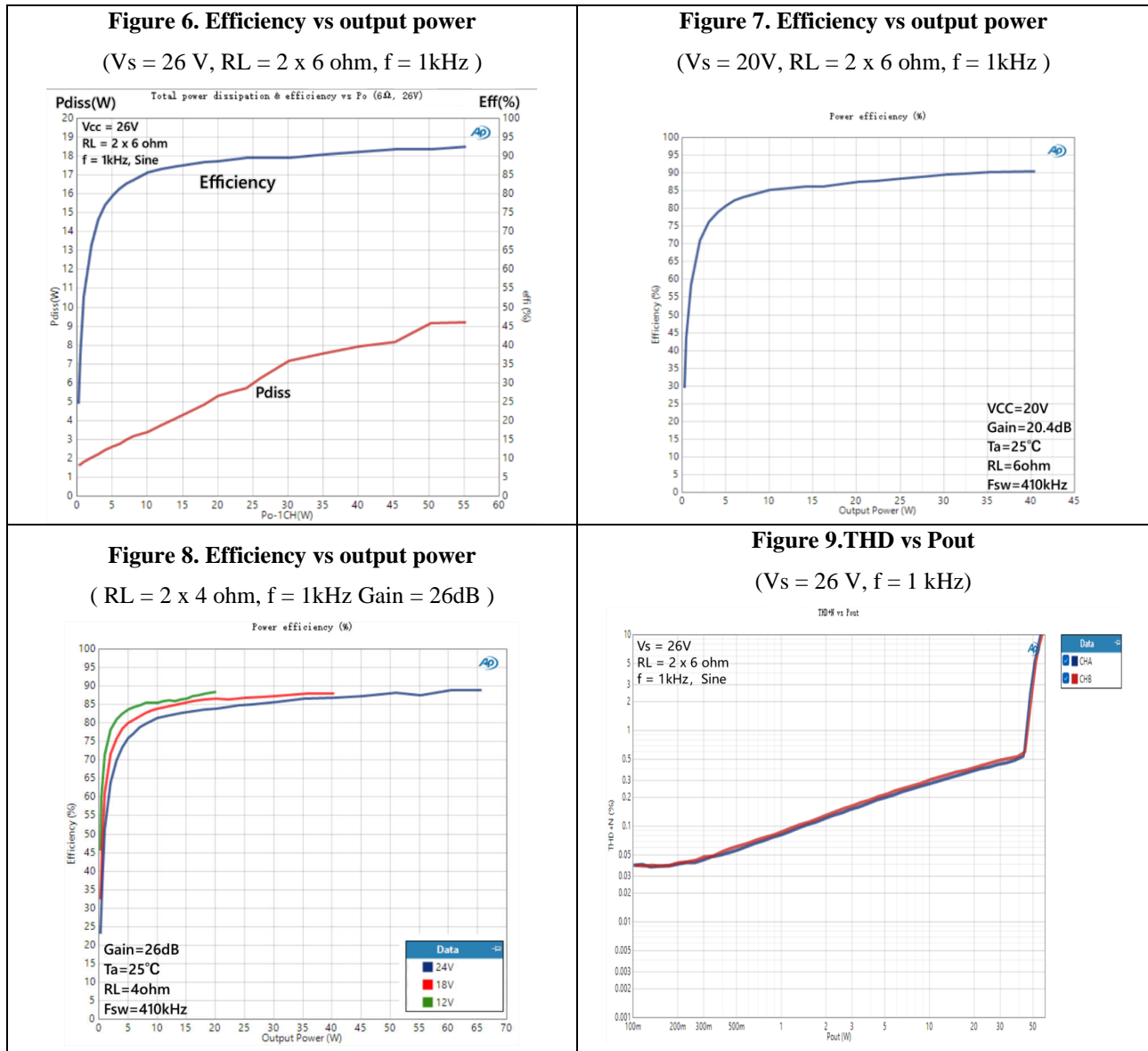
Unless otherwise stated, measurements were made under the following conditions:  $V_{CC} = 26\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $f = 1\text{ kHz}$ ,  $G_v = 32.4\text{ dB}$ ,  $R_{osc} = 39\text{ k}\Omega$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Note: Maximum output power must be derated according to case temperature.

**7.1 Stereo configuration**

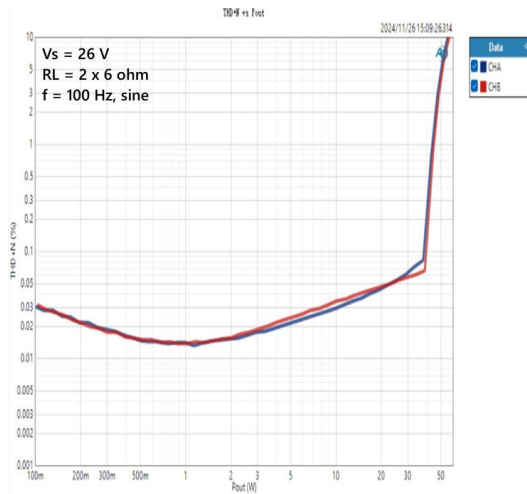
The following characterization curves were made using the SMH7492PE demonstration board (Figure 3: "Application circuit"). The characterization curves were made under the following test conditions:

$V_s = 7$  and  $26\text{ V}$ ,  $R_L = 6\ \Omega$ ,  $R_{osc} = 39\text{ k}\Omega$ ,  $C_{osc} = 100\text{ nF}$ ,  $G_v = 32.4\text{ dB}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$  unless otherwise specified.

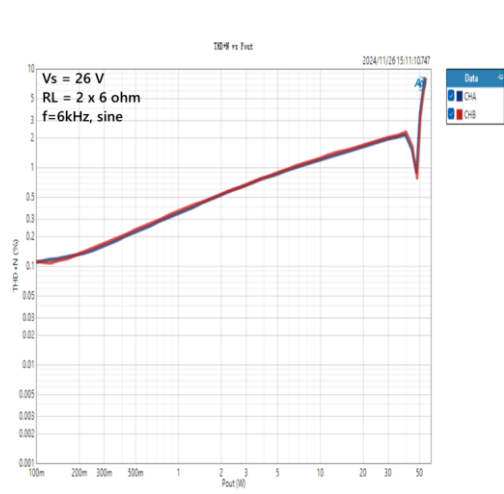


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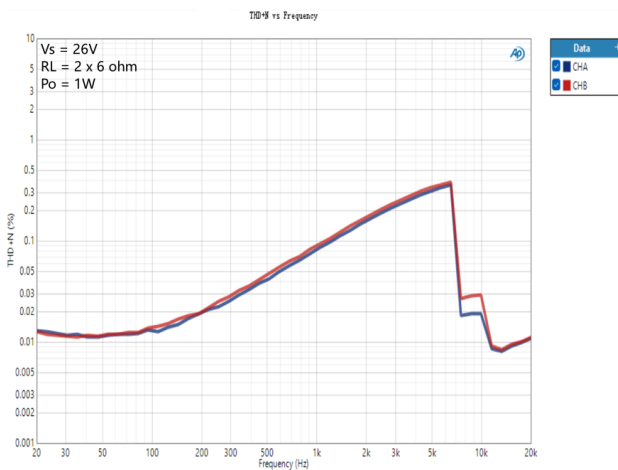
**Figure 10. THD vs Pout**  
(Vs = 26 V, f = 100 Hz)



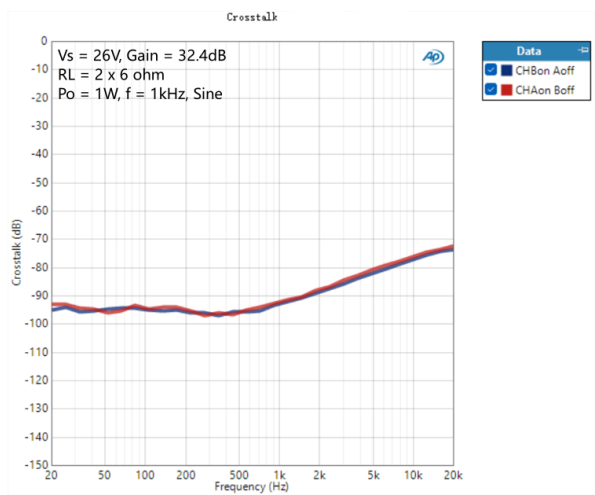
**Figure 11. THD vs Pout**  
(Vs = 26 V, f = 6 kHz)



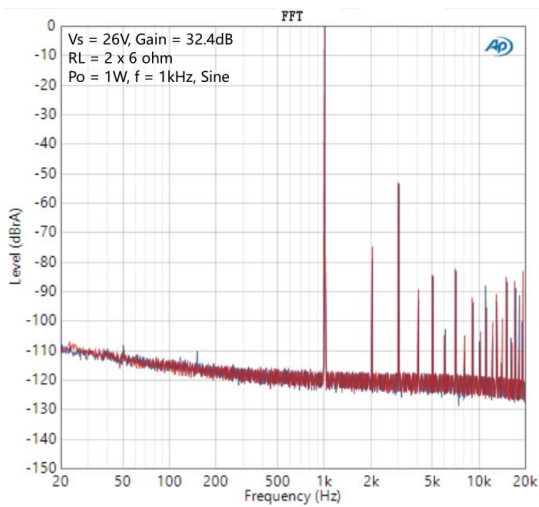
**Figure 12. THD vs frequency**  
(Vs = 26 V, Po = 1 W)



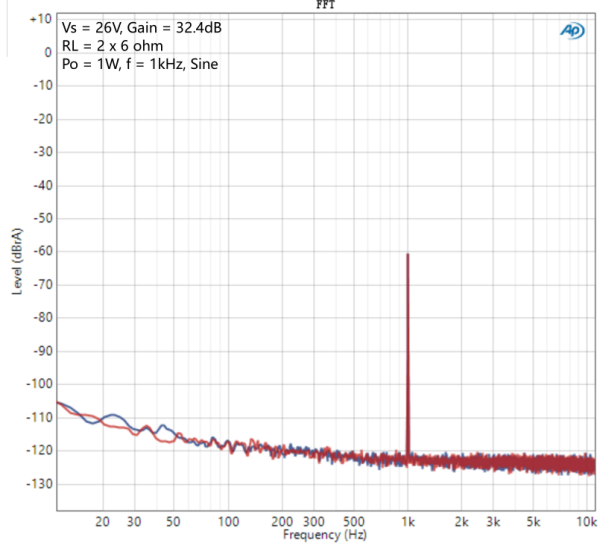
**Figure 13. Crosstalk (Vs = 26 V)**



**Figure 14. FFT (0 dB) (Vs = 26 V)**

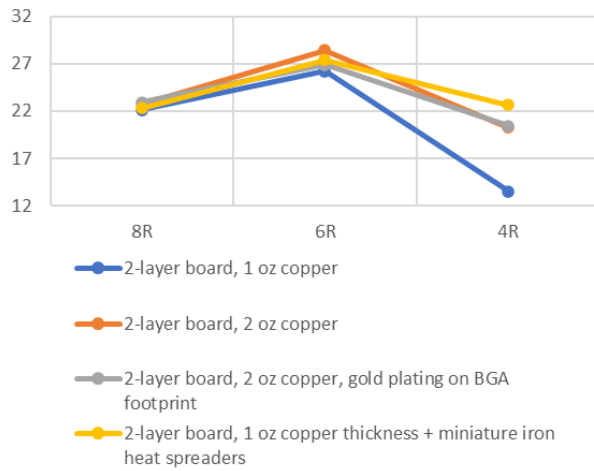


**Figure 15. FFT (-60 dB) (Vs = 26 V)**

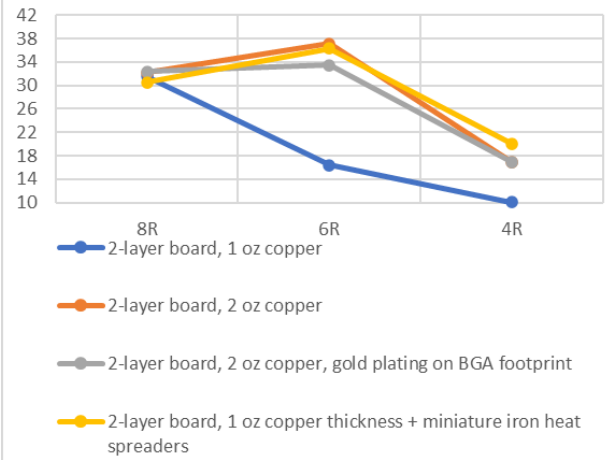


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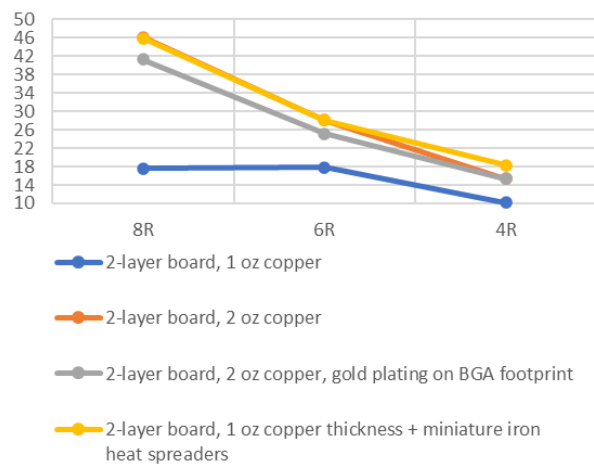
**Figure 16. Maximum Output Power of Different PCB (Vcc=15V)**



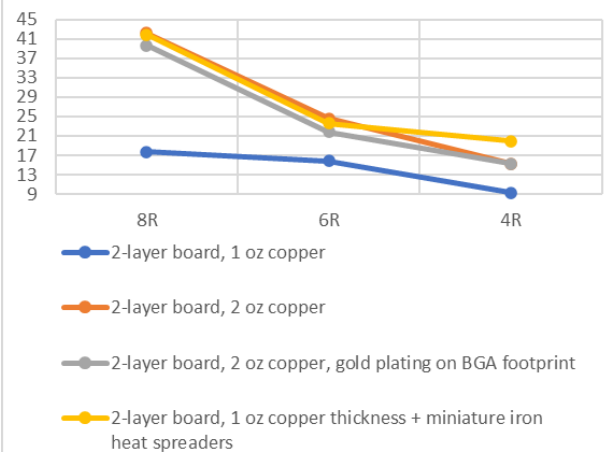
**Figure 17. Maximum Output Power of Different PCB (Vcc=18V)**



**Figure 18. Maximum Output Power of Different PCB (Vcc=22V)**



**Figure 19. Maximum Output Power of Different PCB (Vcc=24V)**



## 8. Applications information

### 8.1 Mode selection

The three operating modes of the SMH7492PE are set by the two inputs STBY (pin 14) and MUTE (pin 15). Standby mode: all circuits are turned off, very low current consumption.

- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

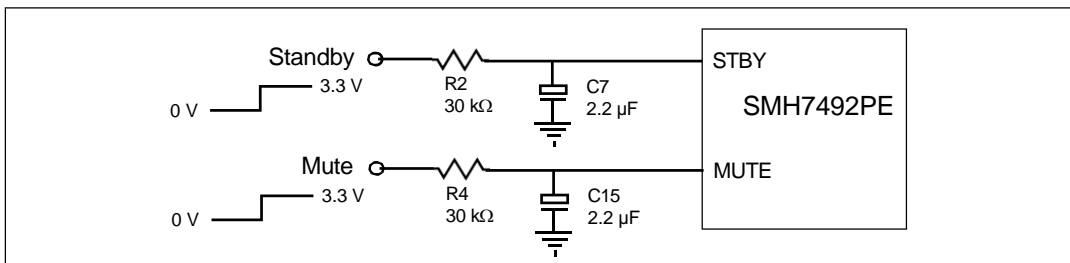
The protection functions of the SMH7492PE are enabled by pulling down the voltages of the STBY and MUTE inputs shown in Figure 20. The input current of the corresponding pins must be limited to 200  $\mu$ A.

**Table 8. Mode settings**

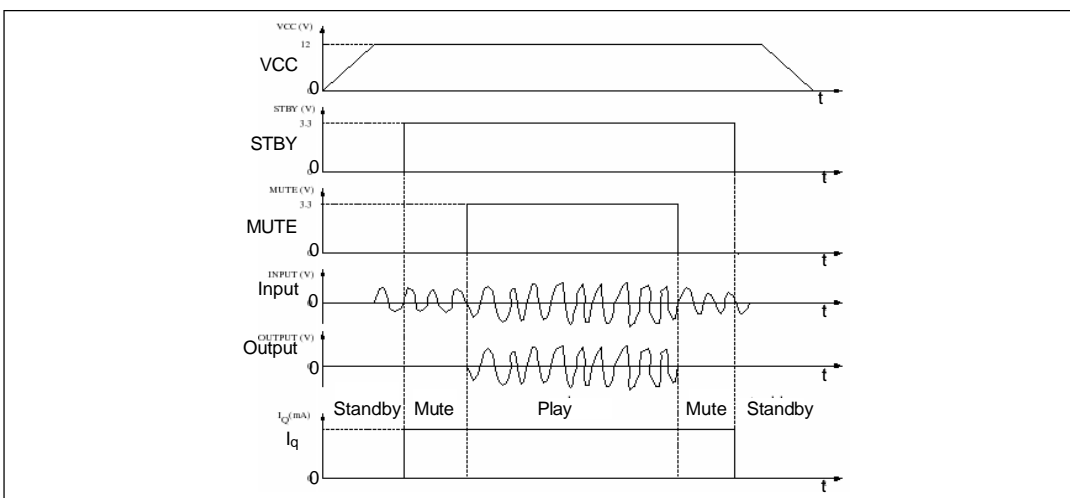
Mode selection	STBY	MUTE
Standby	L <sup>(1)</sup>	X (don't care)
Mute	H <sup>(1)</sup>	L
Play	H	H

1. Drive levels defined in Table 5: Electrical specifications on page 6

**Figure 20. Standby and mute circuits**



**Figure 21. Turn-on/off sequence for minimizing speaker “pop”**





## 8.2 Gain setting

The gain of the SMH7492PE is setting by changing the feedback resistors of the amplifier.

**Table 9. Gain settings**

GAIN	Nominal gain, $G_v$ (dB)
1	32.4
2	29.9
3	26.4
4	20.4

## 8.3 Input resistance and capacitance

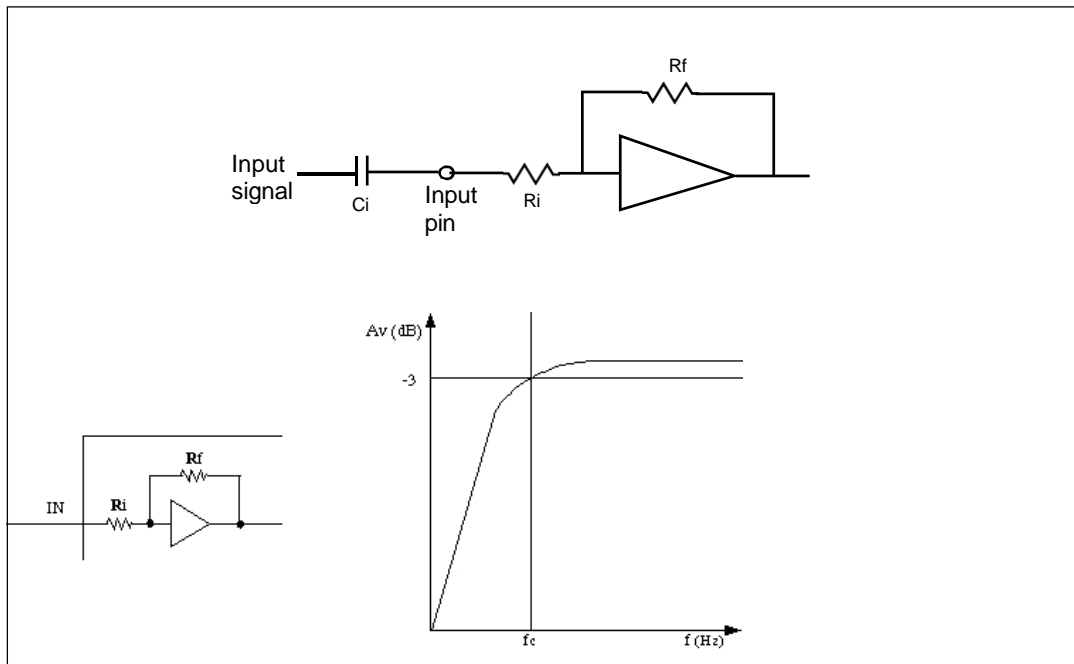
The input impedance is set by an internal resistor  $R_i = 60 \text{ k}\Omega$  (typical). An input capacitor ( $C_i$ ) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in

Figure 22. For  $C_i = 470 \text{ nF}$  the high-pass filter cutoff frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

**Figure 22. Device input circuit and frequency response**



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**8.4 Internal and external clocks**

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one SMH7492PE as master clock, while the other devices are in slave mode (that is, externally clocked). The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

**8.5 Master mode (internal clock)**

Using the internal oscillator, the output switching frequency,  $f_{SW}$ , is controlled by the resistor,  $R_{osc}$ , connected to pin ROsc:  $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$  kHz where  $R_{OSC}$  is in 39 k $\Omega$ .

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:  $f_{SYNCLK} = 2 * f_{SW}$

For master mode to operate correctly then resistor  $R_{osc}$  must be less than 60 k $\Omega$  as given below in Table 10.

**8.6 Slave mode (external clock)**

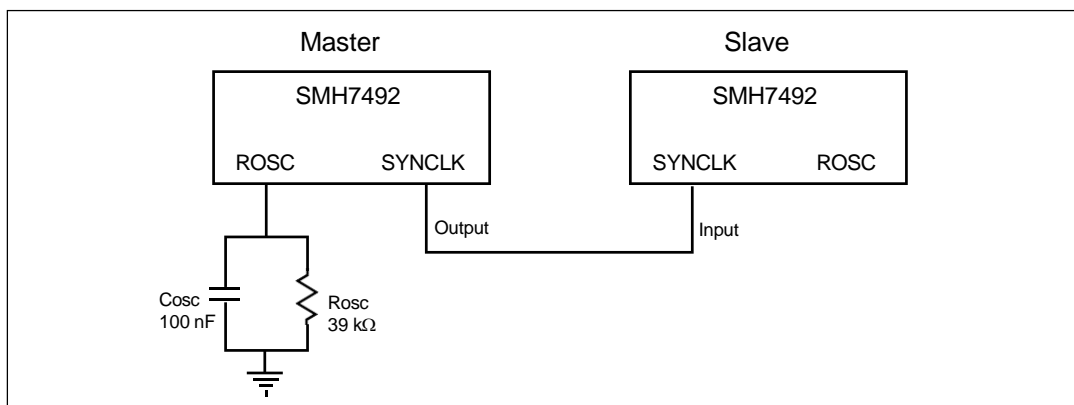
In order to accept an external clock input the pin ROsc must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in Table 10.

The output switching frequency of the slave devices is:  $f_{SW} = f_{SYNCLK} / 2$ .

**Table 10. How to set up SYNCLK**

Mode	ROsc	SYNCLK
Master	$R_{OSC} < 60 \text{ k}\Omega$	Output
Slave	Floating (not connected)	Input

**Figure 23. Master and slave connection**

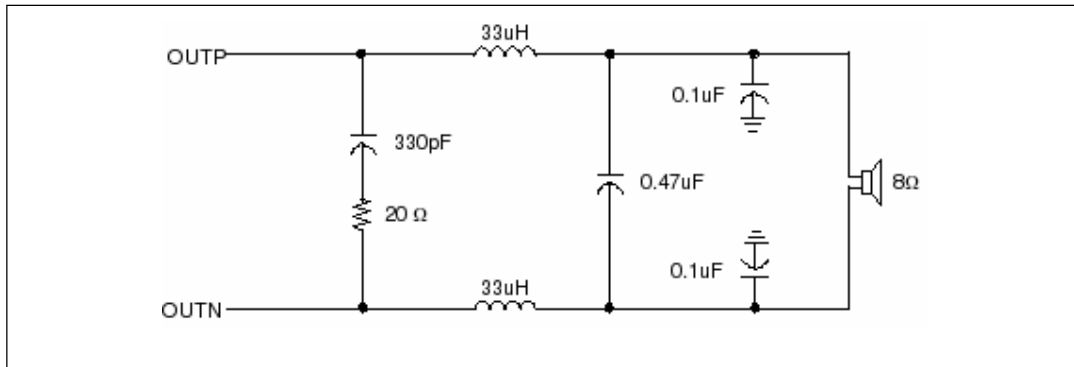


**45 W + 45 W dual BTL class-D audio amplifier**

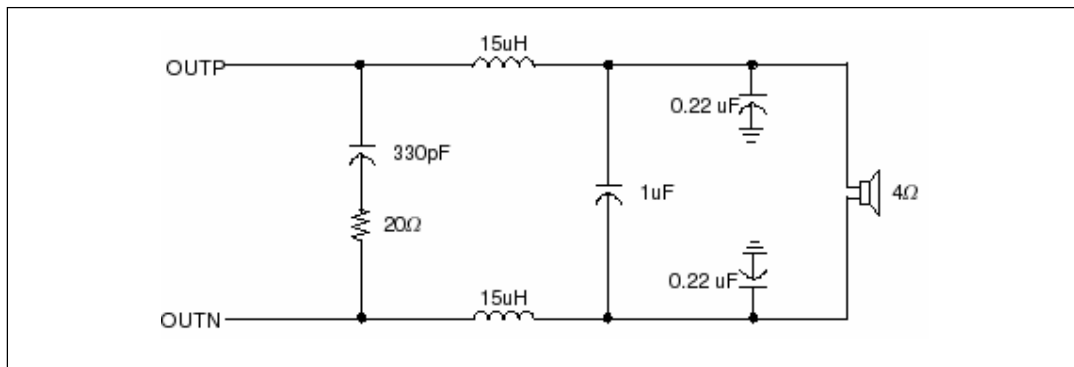
**8.7 Output low-pass filter**

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cutoff frequency of 27 kHz, are shown in Figure 24 and Figure 25 below.

**Figure 24. Typical LC filter for a 8Ω speaker**



**Figure 25. Typical LC filter for a 4Ω speaker**

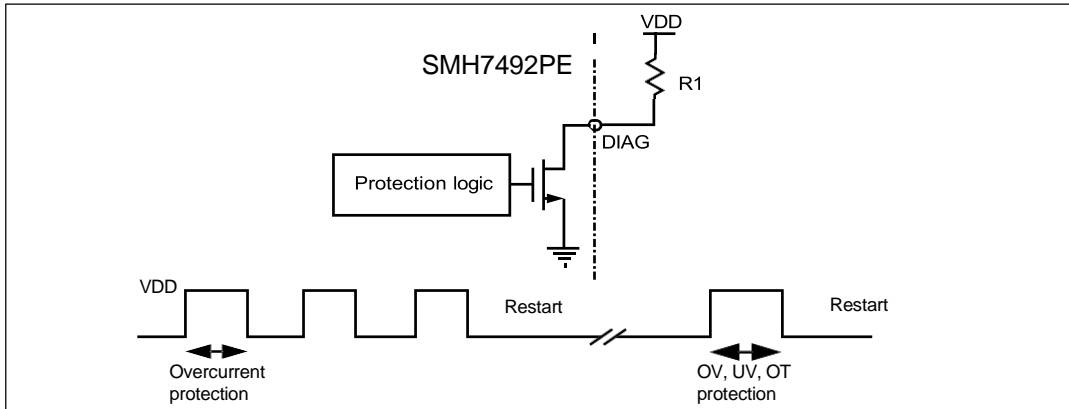


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**8.8 Diagnostic output**

The output pin DIAG is an open-drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<26 V) by a pull-up resistor whose value is limited by the maximum sinking current (200  $\mu$ A) of the pin.

**Figure 26. Behavior of pin DIAG for various protection conditions**



## 9. Protection functions

The SMH7492PE is fully protected against overvoltage, undervoltage, overcurrent and thermal overloads as explained here.

### **Overvoltage protection (OVP)**

If the supply voltage exceeds the value for VOVP given in Table 5: Electrical specifications the overvoltage protection is activated which forces the outputs to the

high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

### **Undervoltage protection (UVP)**

If the supply voltage drops below the value for VUVP given in Table 5: Electrical the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

### **Overcurrent protection (OCP)**

If the output current exceeds the value for IOCP given in Table 5: Electrical specifications the overcurrent protection is activated which forces the outputs to the

high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, TOC, is determined by the R-C components connected to pin STBY.

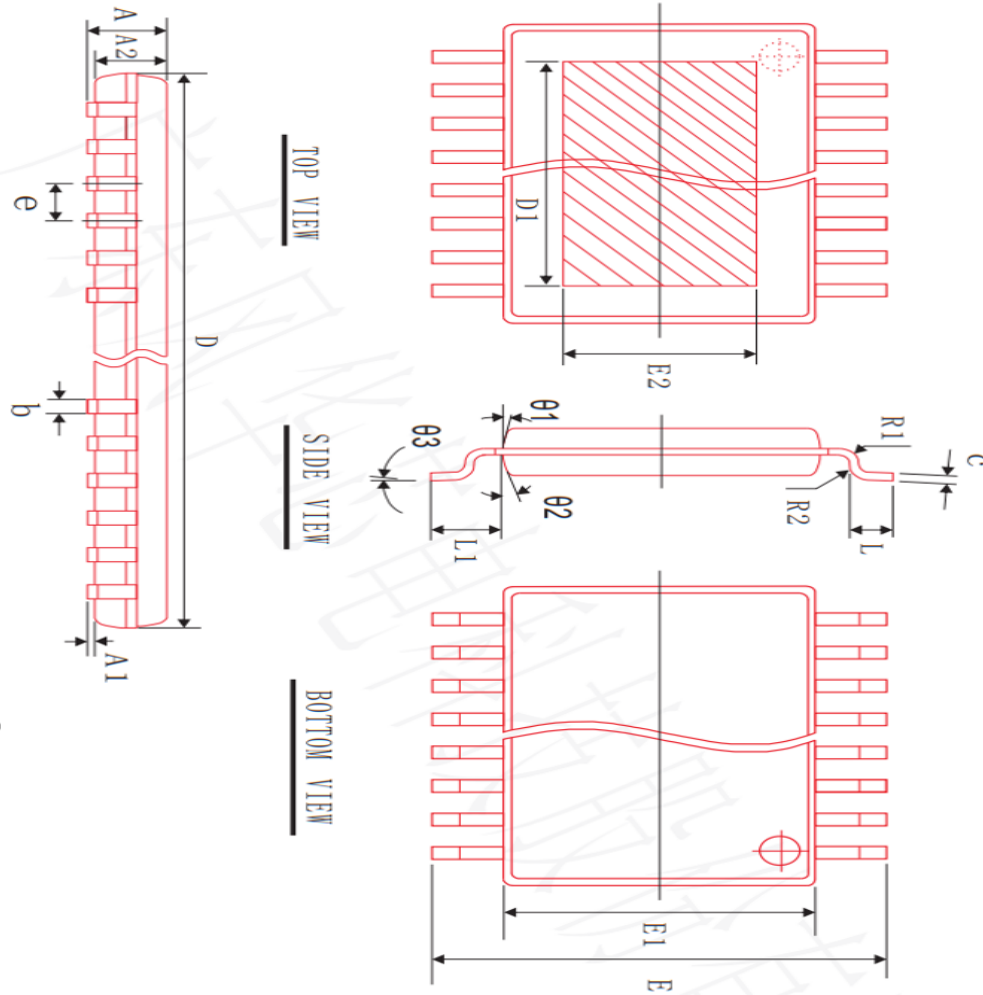
### **Thermal protection (OTP)**

If the junction temperature,  $T_j$ , reaches 145 °C (nominally), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for  $T_j$  given in Table 5: Electrical specifications the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently the device restarts.

## 10. Package mechanical data

The SMH7492PE comes in a 28-pin E-TSSOP28 package with exposed down.

**Figure 27. TSSOP28 package outline**



SYMBOL	MIN	NOM	MAX
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.80	0.875	1.05
C	0.09	0.145	0.20
b	0.19	0.255	0.30
L1	0.95	1.00	1.05
L	0.45	0.60	0.75
D1	5.80	5.90	6.00
E2	2.90	3.00	3.10
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
D	9.60	9.70	9.80
theta3	0	4	8
R1	0.15 TYP		
R2	0.15 TYP		
theta1	0.12° TYP		
theta2	0.12° TYP		
e	0.65 BSC		

COMMON DIMENSIONS  
(UNITS OF MEASURE=mm)

## 11. Revision history

**Table 11.Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
11-Dec-2024	1.0	Initial release.
11-Dec-2024	1.1	Update the Characterization curves
14-Dec-2024	1.2	Add the Parallel information
17-Dec-2024	1.3	Update the Application circuit and the Characterization curves
10-Jan-2025	1.4	Update the Pin list
27-Feb-2025	1.5	Modification the Rdson parameters
4-Mar-2025	1.6	Update the Application circuit
14-Mar-2025	1.7	Added four characteristic curve plots

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