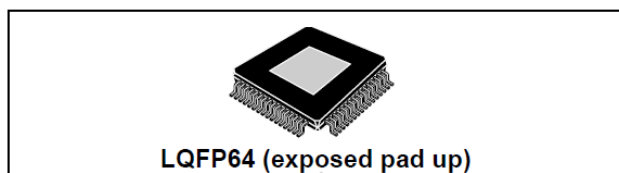


4 × 78W class-D digital input power amplifier with I²C diagnostics and low voltage operation



Features

- AEC-Q100 qualified
- Integrated 120 dB D/A conversion
- I²S and TDM digital input (up to 16 CH TDM)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Class-D channels with 94% efficiency
- EMI control for AM compatibility
- EMI compliance evaluated following normative IEC61967-4 and IEC62132-4
- Low radiation function (LRF)
- Idle tones free DAC
- Output lowpass filter included in the feedback allowing lower cost filter components
- High output power capability
 - 78 W/4 Ω 10% THD, VCC = 25 V
 - 68 W/4 Ω 1% THD, VCC = 25 V
 - 28 W/4 Ω 10 % THD, VCC = 14.4 V
- Full I²C bus driving (3.3/1.8 V):
 - Channels independent tristate
 - Channel independent soft play/mute
 - I²C bus diagnostics, including DC and AC load detection and load value recognition
- Integrated fault protection
- Input and output offset detector
- Clipping detector
- 5.5V operation (“Start-Stop” engines compatibility)
- ESD protection

Description

SMH8081LA is a new BCD technology QUAD BRIDGE class D amplifier, specially intended for automotive applications.

Thanks to the technology used, it is possible to integrate a high-performance D/A converter together with powerful MOSFET outputs in class D, to get an outstanding efficiency compared to the standard class AB.

The integrated D/A converter allows to reach outstanding performances (115 dB SNR with 113 dB of dynamic range). The feedback loop is including the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion independently from the inductor and capacitor quality.

Moreover, SMH8081LA features the most complete diagnostic matrix, including full diagnostic in play to support the most demanding OEM requirements in terms of speaker control and system robustness & reliability. SMH8081LA supports start stop cranking down to 5.5 V.

Order code	SMH8081LA
Qty	1600
Package	LQFP64 (exp. pad up)
Packing	Tray

Contents

1	Block diagram and pins description	3
2	Package information.....	6
2.1	LQFP64 (10x10x1.4 mm exp. pad up)	6
2.2	Generic Package View	7

List of Figures

Figure 1.	Block diagram	3
Figure 2.	Tentative pins connection diagram (top view).....	3
Figure 3.	LQFP64 (10x10x1.4 mm exp. pad up) package information	6
Figure 4.	Generic Package View (top view)	7
Figure 5.	Generic Package View (bottom view)	7

List of Tables

Table 1.	Pins list description.....	4
Table 2.	LQFP64 (10x10x1.4 mm exp. pad up) package information.....	6

1 Block diagram and pins description

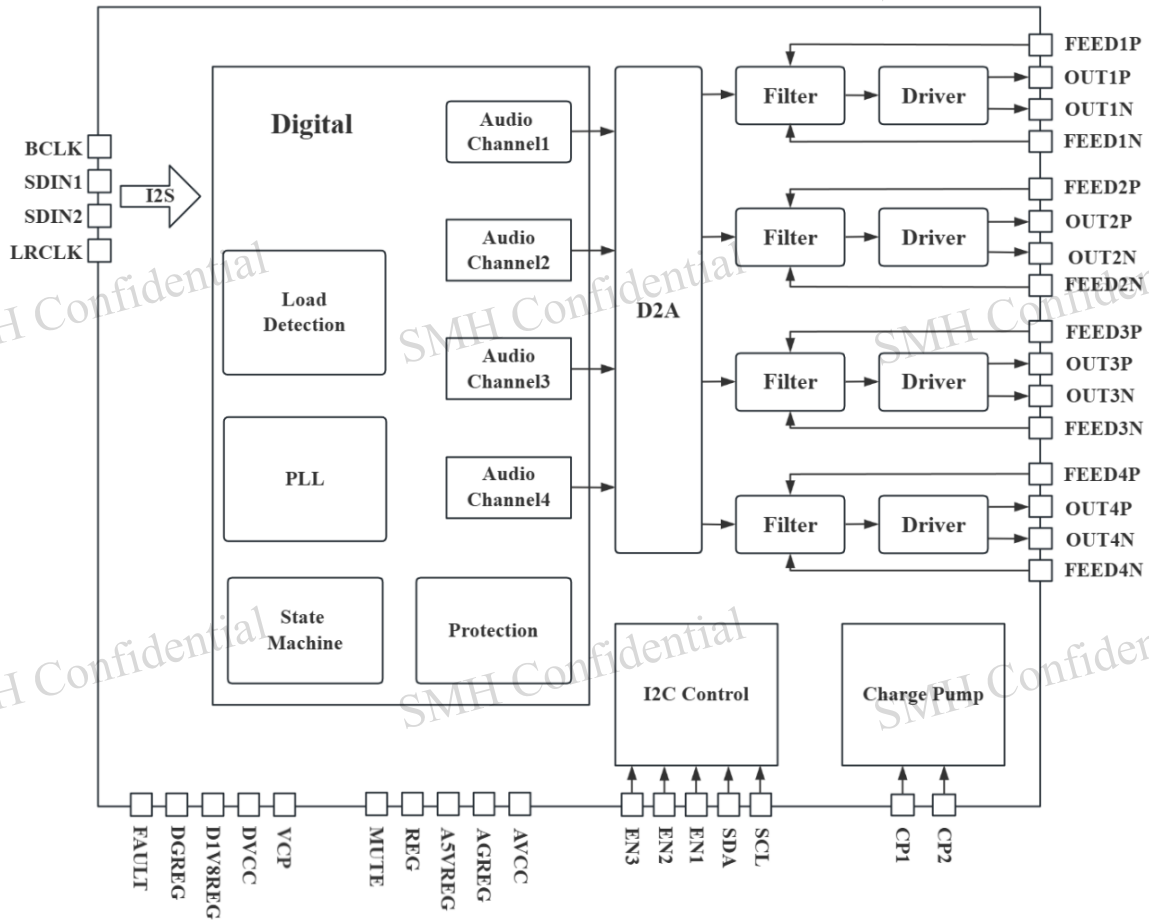


Figure 1. Block diagram

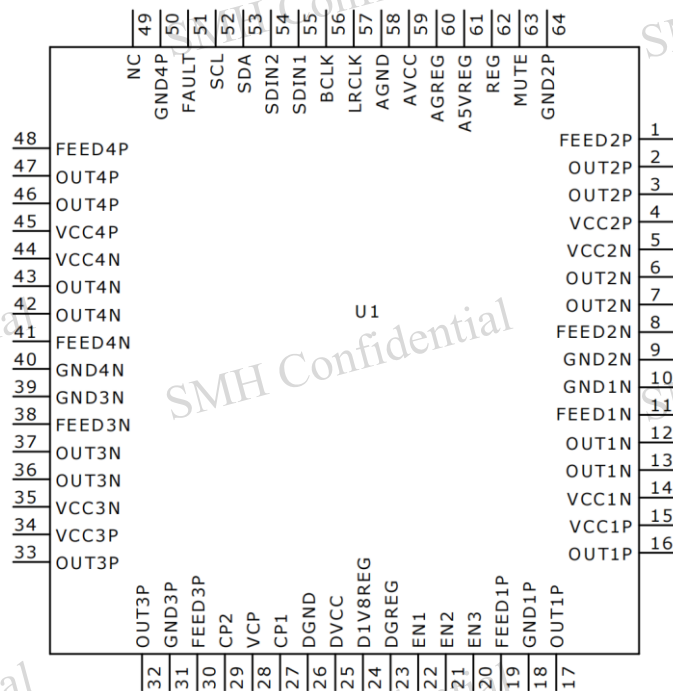


Figure 2. Tentative pins connection diagram (top view)

Table 1. Pins list description

N#	Pin	Function
1	FEED2P	Channel 2, half bridge plus, Feedback
2	OUT2P	Channel 2, half bridge plus, Output
3	OUT2P	Channel 2, half bridge plus, Output
4	VCC2P	Channel 2, half bridge plus, Power Supply
5	VCC2N	Channel 2, half bridge minus, Power Supply
6	OUT2N	Channel 2, half bridge minus, Output
7	OUT2N	Channel 2, half bridge minus, Output
8	FEED2N	Channel 2, half bridge minus, Feedback
9	GND2N	Channel 2, half bridge minus, Power Ground
10	GND1N	Channel 1, half bridge minus, Power Ground
11	FEED1N	Channel 1, half bridge minus, Feedback
12	OUT1N	Channel 1, half bridge minus, Output
13	OUT1N	Channel 1, half bridge minus, Output
14	VCC1N	Channel 1, half bridge minus, Power Supply
15	VCC1P	Channel 1, half bridge plus, Power Supply
16	OUT1P	Channel 1, half bridge plus, Output
17	OUT1P	Channel 1, half bridge plus, Output
18	GND1P	Channel 1, half bridge plus, Power Ground
19	FEED1P	Channel 1, half bridge plus, Feedback
20	EN3	Enable 3
21	EN2	Enable 2
22	EN1	Enable 1
23	DGREG	Negative digital supply V(REG)-0.9V (Internally generated)
24	D1V8REG	Positive digital supply V(REG)+0.9V (Internally generated)
25	DVCC	Digital supply
26	DGND	Digital ground
27	CP1	Charge Pump pin1
28	VCP	Charge Pump output voltage
29	CP2	Charge Pump pin2
30	FEED3P	Channel 3, half bridge plus, Feedback
31	GND3P	Channel 3, half bridge plus, Power Ground
32	OUT3P	Channel 3, half bridge plus, Output
33	OUT3P	Channel 3, half bridge plus, Output
34	VCC3P	Channel 3, half bridge plus, Power Supply
35	VCC3N	Channel 3, half bridge minus, Power Supply
36	OUT3N	Channel 3, half bridge minus, Output

N#	Pin	Function
37	OUT3N	Channel 3, half bridge minus, Output
38	FEED3N	Channel 3, half bridge minus, Feedback
39	GND3N	Channel 3, half bridge minus, Power Ground
40	GND4N	Channel 4, half bridge minus, Power Ground
41	FEED4N	Channel 4, half bridge minus, Feedback
42	OUT4N	Channel 4, half bridge minus, Output
43	OUT4N	Channel 4, half bridge minus, Output
44	VCC4N	Channel 4, half bridge minus, Power Supply
45	VCC4P	Channel 4, half bridge plus, Power Supply
46	OUT4P	Channel 4, half bridge plus, Output
47	OUT4P	Channel 4, half bridge plus, Output
48	FEED4P	Channel 4, half bridge plus, Feedback
49	NC	Device slug connection
50	GND4P	Channel 4, half bridge plus, Power Ground
51	FAULT	Clipping detector and diagnostic output pin: – Overcurrent protection intervention – Thermal warning – Offset detection
52	SCL	I ² C Clock
53	SDA	I ² C Data
54	SDIN2	I ² S /TDM Data input 2
55	SDIN1	I ² S /TDM Data input 1
56	BCLK	I ² S /TDM Clock input
57	LRCLK	I ² S /TDM Sync input
58	AGND	Analog ground
59	AVCC	Analog supply
60	AGREG	Negative Analog Supply V(REG)-2.5V (Internally generated)
61	A5VREG	Positive Analog Supply V(REG)+2.5V (Internally generated)
62	REG	Supply Voltage Ripple Rejection Capacitor
63	Mute	Hardware MUTE pin
64	GND2P	Channel 2, half bridge plus, Power Ground

2 Package information

2.1 LQFP64 (10x10x1.4 mm exp. pad up)

**Table 2. LQFP64
(10x10x1.4 mm exp. pad
up) package information**

Sym	Dimension(mm)		
	Min	Nom	Max
A			1.49
A1	-0.05		0.05
A2	1.35	1.40	1.45
b			0.27
b1	0.17	0.20	0.23
c	0.09		0.20
c1	0.09	0.127	0.16
D1	9.90	10.00	10.10
E1	9.90	10.00	10.10
e	0.50 BSC		
D	11.90	12.00	12.10
D2	6.40	6.50	6.60
E	11.90	12.00	12.10
E2	6.40	6.50	6.60
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20		
θ	0°	3.5°	6°
θ 1	0°		
θ 2	12° REF		
θ 3	12° REF		
R1	0.08		
R2	0.08		0.20
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		

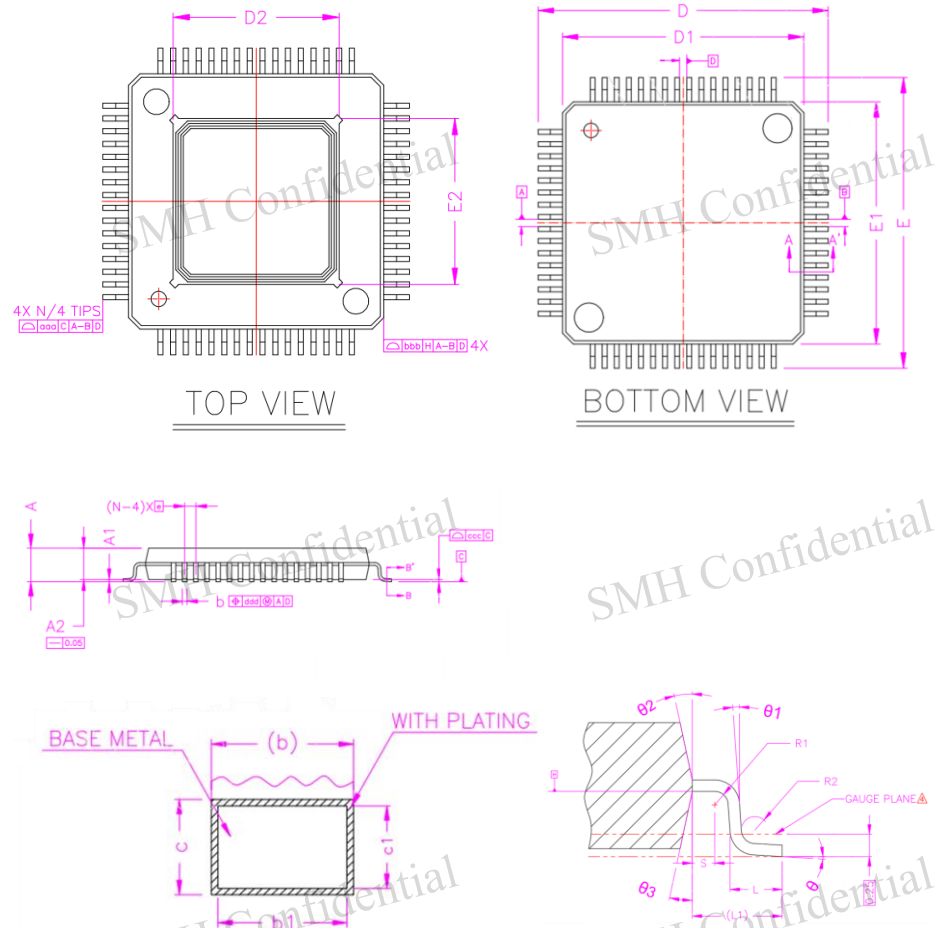


Figure 3. LQFP64 (10x10x1.4 mm exp. pad up) package information

- 1) Refer to JEDEC STD. MS-026 Issue. D
- 2) Dimension D1 and E1 do not include mold protrusion.
Allowable mold flash or protrusion is 0.25 mm per side.
D1 and E1 are maximum plastic body size dimension include mold mismatch.
- 3) Dimension b does not include dambar protrusion.
Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.
- 4) All dimensions are in millimeters.

2.2 Generic Package View

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

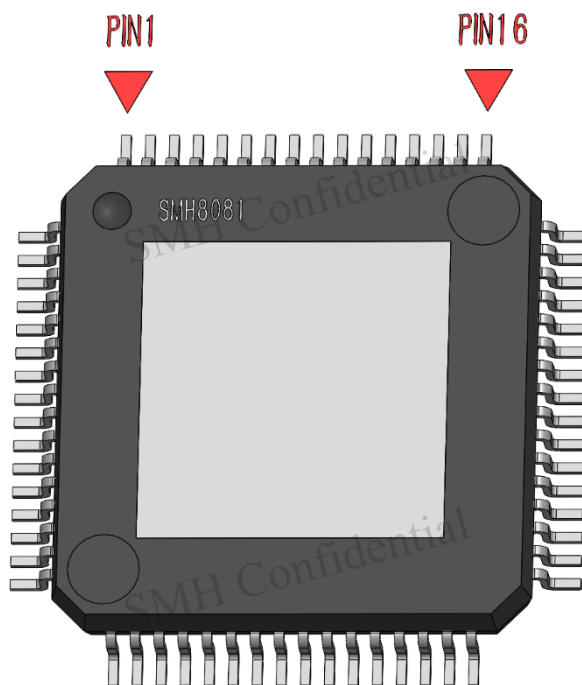


Figure 4. Generic Package View (top view)

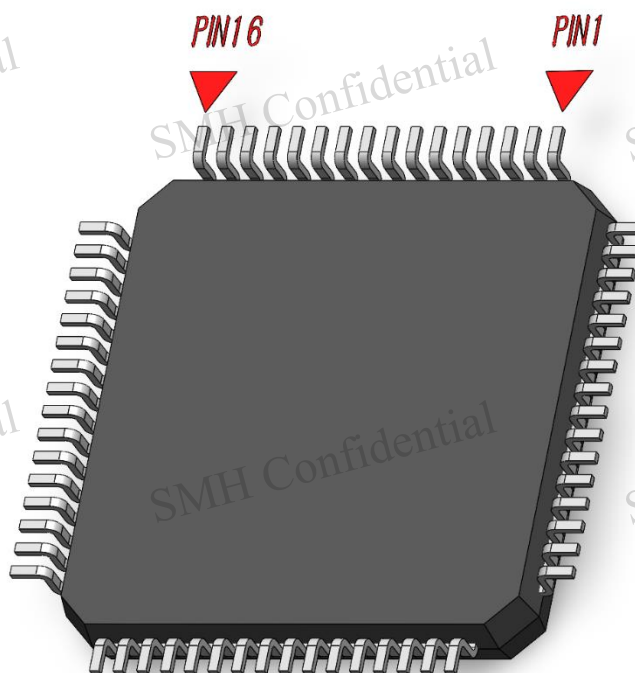


Figure 5. Generic Package View (bottom view)