# Support Plus PD-LINK USB Double ports Controller

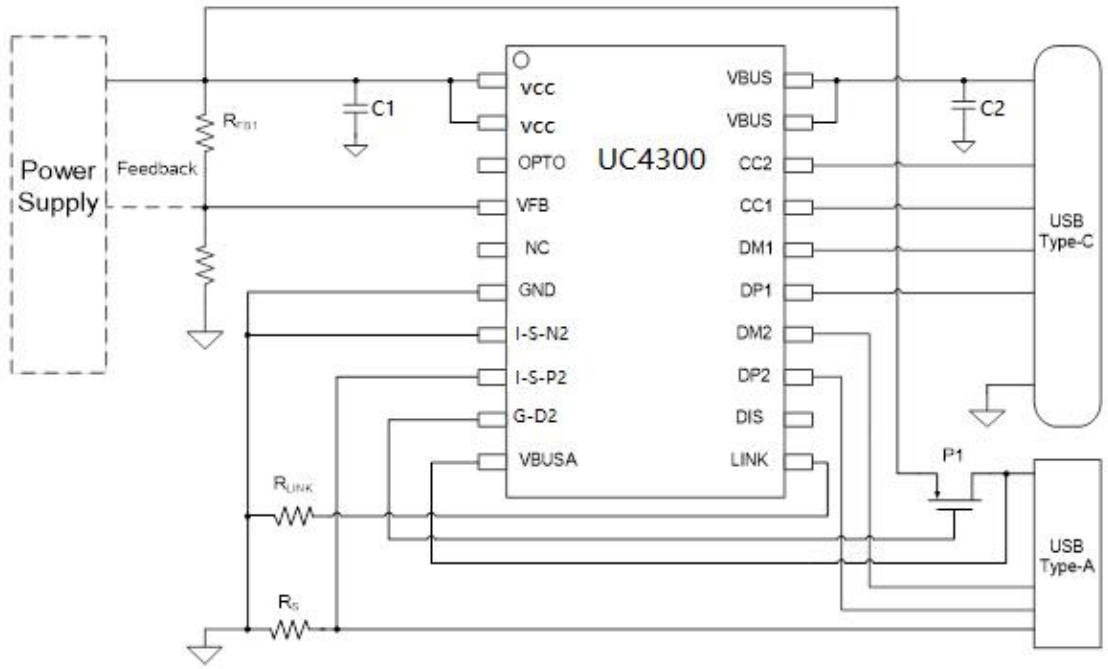
## Feature

- Support USB type-C protocol
  -Configure as DFP (source)
  -Broadcast 3A /1.5A current
- Support USB power delivery (PD) 2.0 and 3.0 and PPS protocol ---Integrated PD layered
- communication protocol
  -PDO configurable: 5V, 9V, 12V, 15V,
  -Apdo configurable: 5V prog, 9V prog,
- Support quick charge 3.0 /2.0 protocol
  -Configurable Xiaomi 27W charge Turbo
- Support Huawei FCP / SCP protocol
- Support Samsung AFC protocol
- Support USB BC1.2 DCP
- Support apple 2.4A charging
- Specification
- Integrated constant voltage (CV) compensation loop
  Integrated VBUS channel low impedance power switch
- built in VBUS discharge function
- Support line loss compensation function
- Support USB type
  -A and type-C dual port operation mode
  - fast charging when port A or port C works independently
  - when the A port is connected to the apple charging cable but not connected to the apple mobile phone, the C port still has fast charging
  - when there are equipment access to port A and port C at the same time, it works at 5V
- Safety
  - the type-A port is controlled by the switch at the power end to avoid the leakage caused by the short circuit
  - overvoltage / undervoltage protection
  - over current protection
  -Over temperature protection
- CC1 / CC2 / DP / DM overvoltage protection
- ESD characteristics ± 4KV
- Package: TSSOP-20

## Application

- AC-DC adapter
- USB Adapter

## Application Circuit



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# DESCRIPTION

UC4300 is A multi-functional USB dual port controller integrating USB type-C, USB power delivery (PD) 2.0/3.0 and PPS, qc3.0/2.0 class B fast charging protocol, Huawei FCP / SCP fast charging protocol, Samsung AFC fast charging protocol, BC1.2 DCP and Apple device 2.4A charging specification, Provide complete type-C and type-a dual port charging solutions for AC-DC adapter, mobile power supply, car charger and other equipment.

UC4300 is specially integrated with plus PD-link Gamma Internet patent technology. Through plus PD-link Gamma With the interconnection function, UC4300 can be easily and flexibly applied in the charging scheme of multiple type-C and type-a ports.

The built-in type-C protocol of UC4300 can support the type-C device to be inserted into the Automatic wake-up system, identify the plug forward and reverse, and realize the connection. The integrated type-C pd3.0 protocol supports bi-directional mark coding (BMC), integrates the physical layer protocol and protocol engine of hardware, and does not need software to participate in encoding and decoding.

When one of the type-C and type-a ports is connected to the device, the type-C or type-A port can realize independent fast charging function. When both type-C and type-A are connected to the device, UC4300 will reduce the output voltage to 5V to supply power to the device. In particular, when the type-A port is always connected to the apple charging cable but not connected to the Apple phone, the type-C port still has the fast charging function. When used as A charger, the charging line is often connected to the charger. UC4300 perfectly solves the problem of fast charging when type-A and type-C port are connected with charging line. UC4300 built in A variety of protection mechanisms to ensure the safety of the equipment: including dynamic overvoltage / under voltage / overcurrent protection (the protection point can be adjusted according to the proportion of the working voltage / current requested by the equipment); start monitoring (the port voltage will be monitored before VBUS output). UC4300 integrates 25m Ω VBUS channel power switch and internal discharge channel, which saves peripheral devices and can quickly turn off output and restore to safe state in case of error.

UC4300 is packaged in TSSOP20.

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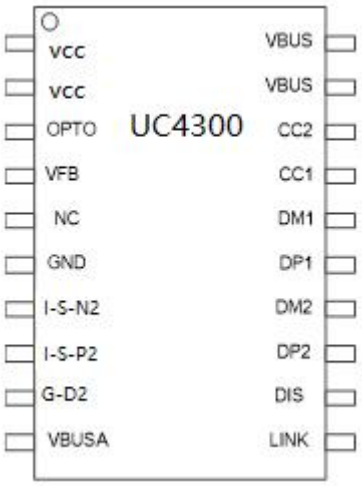
## Pin function




| PIN | NAME | Description |
|---|---|---|
| 1/2 | VCC | Source INPUT |
| 3 | OPTO | OPTO coupler driver |
| 4 | VFB | Voltage adjust feedback connection |
| 5 | NC | No connection |
| 6 | GND | GND |
| 7 | I-S-N2 | Type-A port, current sense negative port |
| 8 | I-S-P2 | Type-A port, current sense positive port |
| 9 | G-D2 | Type-A port, PMOS Switch driver |
| 10 | VBUS-A | Type-A port, output VCC |
| 11 | LINK | Plus PD-LINK™ Port |
| 12 | DIS | Control the discharge MOS gate |
| 13 | DP2 | Type-A Port DP |
| 14 | DM2 | Type-A Port DM |
| 15 | DP1 | Type-C Port DP |
| 16 | DM1 | Type-C Port DM |
| 17 | CC1 | Type-C Port CC1 |
| 18 | CC2 | Type-C Port CC2 |
| 19 | VBUS | VBUS output |
| 20 | VBUS | VBUS output |

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# Order Information

| name | PDO And APDO Configuration | mark | package |
|---|---|---|---|
| UC4300 | High power Output PDO : 5V/3A, 9V/3A, 12V/2.25A, 9V/2.2A（Apple 20W）<br>Low power output PDO : 5V/2A | UC4300 | TSSOP20 |

Mark information：

Line 1，UC4300：Chip mark；

Line 2，XXXXX：Lot Number;

# Available function

| | QC3.0 | FCP/SCP | AFC | PD3.0 | PPS | A+C | Plus PD-link |
|---|---|---|---|---|---|---|---|
| UC4300 | Y | Y | Y | Y | Y | Y | Y |

# Specifications

## Absolute Maximum Ratings

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| Broken Voltage(VS to GND） | VIN, VCC, PS, CC, VBUS, OPTO, DP, DM | -0.3 | 24 | V |
| | The others Pin | -0.3 | 6 | V |
| Operating Junction Temperature Range | | -40 | 150 | ℃ |
| Storage Temperature | | -65 | 150 | ℃ |

(1) Absolute maximum ratings are stress limits beyond which damage to the device may happen.。

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## ESD feature

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{ESD}$ | HBM | ±4000 | V |

## Recommended operating conditions

| Parameter | | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| VCC | Input voltage | 3.6 | | 15 | V |
| $C_{VBUS}$ | Discharge limitation resistor | 2.2 | | 10 | μF |
| $C_{VCC}$ | VAUX Capacitor | 4.7 | 10 | | μF |
| $R_{FBUP}$ | VBUS Capacitor | | 100 | | kΩ |
| $T_A$ | System voltage divider resistor | -40 | | 85 | ℃ |

## Package thermal Data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Max Junction-to-Ambient Thermal Resistance (1) | 100 | ℃/W |
| $R_{\theta JCtop}$ | Max Junction-to-Case Thermal Resistance | 36 | |
| $R_{\theta JB}$ | Thermal resistance between junction and plate temperature | 45 | |

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# ELECTRICAL CHARACTERISTICS

(T$_J$= 25℃，5V≤VCC≤12V , unless otherwise specified)

| Parameter | | Test conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VCC，VBUS** | | | | | | |
| $V_{VCC\_TH}$ | VCC UVLO Threshold | Rising edge | | 3.3 | | V |
| | | Falling edge | | 2.9 | | |
| | | Hysteresis | | 0.4 | | |
| $I_{SUPP}$ | Operating current | VCC=5V，VBUS=5V | | 2 | | mA |
| **Voltage Protection (VBUS)** | | | | | | |
| $V_{FOVP}$ | Fast OVP Threshold，always enabled | Ref to target voltage | | +20% | | V |
| $V_{SOVP}$ | Slow OVP Threshold | Ref to target voltage | | +15% | | V |
| $V_{SUVP}$ | VBUS UVP Threshold | Ref to target voltage | | -22% | | V |
| **Switch MOSFET** | | | | | | |
| $R_{DSON}$ | | | | 25 | | mΩ |
| **Transmitter (CC1, CC2)** | | | | | | |
| $R_{TX}$ | Output resistance | During transmission | | 50 | | Ω |
| $V_{TXHI}$ | Transmit HIGH | | | 1.15 | | V |
| $V_{TXLO}$ | Transmit LOW | | -75 | | 75 | mV |
| $t_{UI}$ | Bit unit interval | | | 3.3 | | us |
| $t_{BMC}$ | Rise/fall time of BMC | $R_{load}$=5.1k,$C_{load}$=1nF | 300 | | 600 | ns |
| **Receiver (CC1, CC2)** | | | | | | |
| $V_{RXHI}$ | Receive HIGH | | 800 | 840 | 885 | mV |
| $V_{RXLO}$ | Receive LOW | | 485 | 525 | 570 | |
| $I_{RP\_SRC}$ | CC1/CC2 Broadcasting current | 3A DFP mode, 0 ≤ $V_{CCX}$ ≤ 2.5V | 304 | 330 | 356 | uA |
| | | 1.5A DFP mode, 0 ≤ $V_{CCX}$ ≤ 1.5V | 166 | 180 | 194 | uA |
| **OCP** | | | | | | |
| $V_{ITRIP}$ | | Ref to Power Capability(pd) | | +30% | | A |
| | | USB-A | | | | A |
| **OTP (internal)** | | | | | | |
| $T_{J1}$ | Die temperature | Temperature rising edge | 135 | 145 | 155 | ℃ |
| | | Hysteresis | | 20 | | ℃ |
| **HVDCP interface (DP, DM)** | | | | | | |
| $V_{DAT(REF)}$ | Data line detection voltage | | 0.25 | 0.325 | 0.4 | V |

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| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{SEL(REF)}$ | Output voltage selection | | 1.8 | 2 | 2.2 | V |
| $T_{GLITCH(DP)HIGH}$ | D+ High level disturbance filtering time | | 1 | 1.25 | 1.5 | s |
| $T_{GLITCH(DM)LOW}$ | D- Low level disturbance filtering time | | | 1 | | ms |
| $T_{GLITCH(V)CHANGE}$ | Output voltage disturbance filtering time | | 20 | 40 | 60 | ms |
| $T_{GLITCH(CONT)CHANGE}$ | Disturbance filtering time in continuous mode | | 100 | 150 | 200 | us |
| $R_{DAT(LKG)}$ | D+ Leakage resistance | | 300 | 500 | 800 | KΩ |
| $R_{DM(DWN)}$ | D- DroPD-outputwn resistance | | 14.25 | 19.53 | 24.5 | KΩ |
| $R_{ON(N1)}$ | Switch N1 on resistance | | | 40 | 100 | Ω |
| $V_{TH(PD)}$ | Connection voltage threshold of receiving device | | 0.25 | 0.325 | 0.4 | V |
| $TD_{PD}$ | Connection detection and filtering time for receiving equipment | | 120 | 160 | 200 | ms |
| $\Delta I_{T(UP)}$ | Step size of current source when voltage rises | $R_{IREF}$=100KΩ | | 2 | | uA |
| $\Delta I_{T(DO)}$ | Step size of current source when voltage is reduced | $R_{IREF}$=100KΩ | | 2 | | uA |
| **Apple 2.4A Charge mode** | | | | | | |
| $V_{DAT(2.7V)}$ | D+/D- voltage | | 2.57 | 2.7 | 2.84 | V |
| $R_{DAT(2.7V)}$ | D+/D- output impedance | | | 15 | | KΩ |
| **FCP charge mode** | | | | | | |
| $V_{TX-VOH}$ | D- FCP TX Valid High | | | 2.7 | | V |
| $V_{TX-VOL}$ | D- FCP TX Valid Low | | | | 0.3 | V |
| $V_{RX-VIH}$ | D- FCP RX Valid High | | | 1.2 | | V |
| $V_{RX-VIL}$ | D- FCP RX Valid High | | | 0.9 | | V |
| Trise | FCP Pulse Rise Time | 10% - 90% | | | 2.5 | us |
| Tfall | FCP Pulse Fall Time | 90% - 10% | | | 2.5 | us |

# Application informatin

## VCC 和 VBUS

VCC is the input power of type-C and type-a ports. It is used as the power input of VBUS and the power supply pin of the chip to connect the output of ACDC or DCDC. It is recommended to connect GND to 2 ~ 10uF ceramic capacitor near VCC and VBUS pins.

## OPTO

OPTO is used to Drive Optocoupler, with withstand voltage of more than 24V (see application diagram in Chapter 3).

VFB

VFB and OPTO form CV loop, which needs to be compensated. The reference at VFB is 1.24v, and the partial voltage resistance near VCC must be 100k, and the other is 33K (corresponding to VCC = 5V); the resistance accuracy affects the power supply accuracy, so it is recommended to use 1% accuracy resistance.

Current Sense

UC4300 has two sets of current detection circuits, corresponding to port C and port A respectively. Port C current detection is completely built-in, and the default protection point is 130% of PDO current; port A current protection points are 2.8/3.2/3.6/4a optional (use 10m Ω to detect resistance). The detection resistance of 10m Ω needs to be connected by Kelvin, one end is ISP2, the other end is the GND of the chip.

Line loss compensation

UC4300 can increase the output voltage in proportion according to the load current (60 / 90 / 120mV /A optional), and can also offset the output voltage in A fixed way (- 150mV ~ + 400mV).

Multi-port Applications

UC4300 can realize fast charging in single port application, and it will return to 5V charging when A + C works at the same time; moreover, it can realize whether the apple cable or mobile phone is connected to port A through special technology to avoid affecting the quick charging of port C when there is only apple cable in port a.

Safety characteristics

Withstand voltage

In order to avoid chip damage caused by CC / DP / DM pin and power short circuit, the withstand voltage of these ports can reach more than 24V.

OVP/OCP/UVP

The chip OVP/OCP/UVP threshold will be adjusted according to the voltage selected by the device to protect the device security to the maximum extent.

OTP

When the chip junction temperature reaches 145 ℃, the output will be closed, and when it drops to 125 ℃, it will be released.。

Discharge

UC4300 has built-in energy discharge channel, which can open the discharge power energy under specific circumstances。

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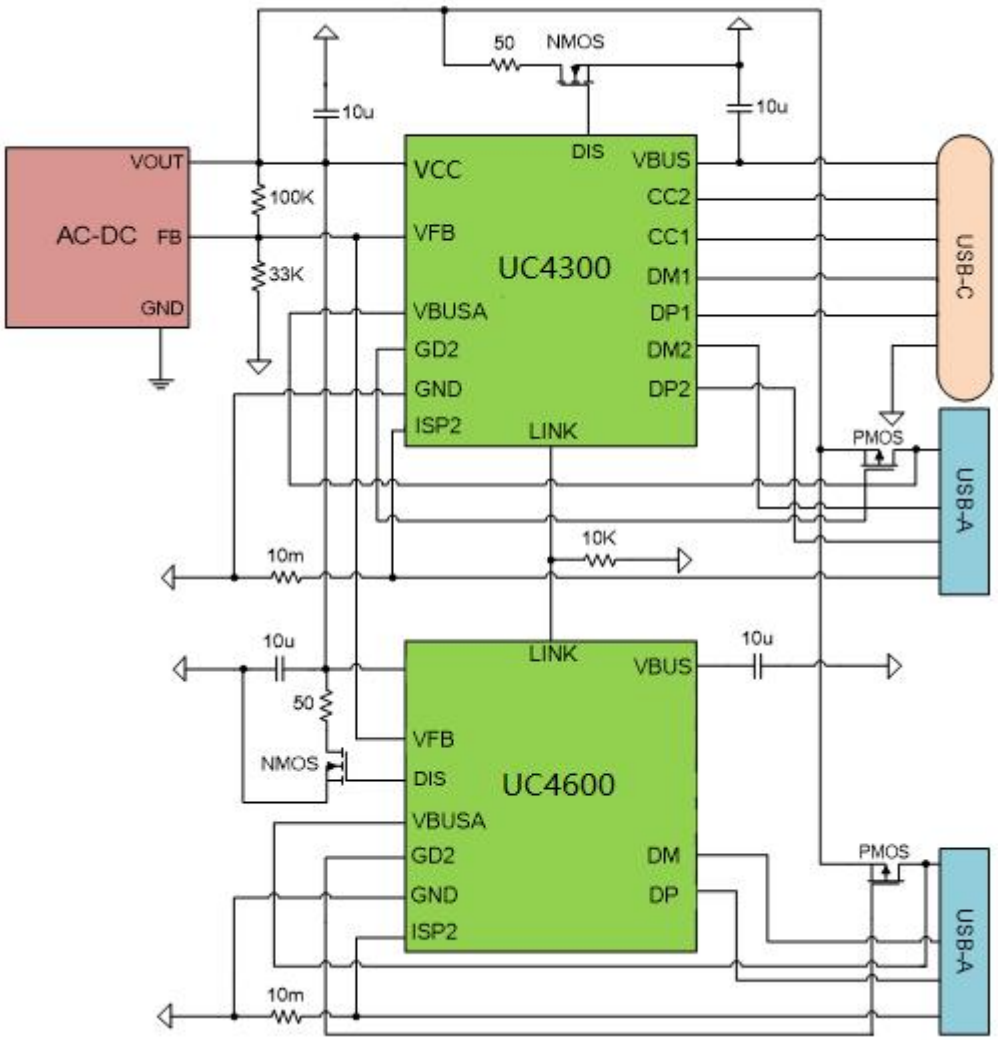
## 2A+1C application:




UC4300+UC4600: 2A+1C application

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## Package Information

| 尺寸 / 标注 | 最小（mm） | 最大（mm） | 尺寸 / 标注 | 最小（mm） | 最大（mm） |
|---|---|---|---|---|---|
| A | 6.40 | 6.60 | C3 | 0.05 | 0.15 |
| A1 | 0.20 | 0.30 | D | 1.0TYP | |
| A2 | 0.65TYP | | D1 | 0.50 | 0.75 |
| B | 6.30 | 6.50 | R1 | 0.15TYP | |
| B1 | 4.30 | 4.50 | R2 | 0.15TYP | |
| C | 0.90 | 1.05 | θ1 | 12° TYP | |
| C1 | 0.4365TYP | | θ2 | 12° TYP | |
| C2 | 0.09 | 0.2 | θ3 | 0° TYP | 8° TYP |
| | | | θ4 | 10° TYP | |